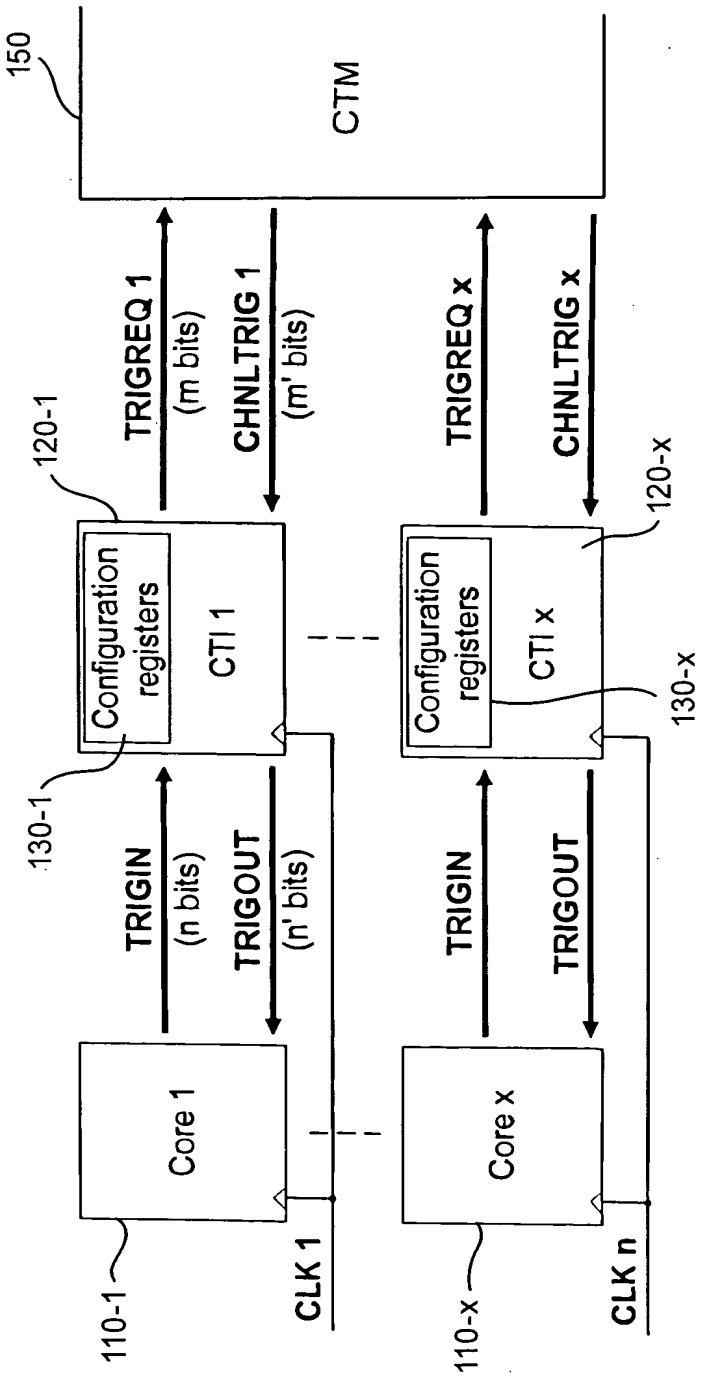

FIGURE 1

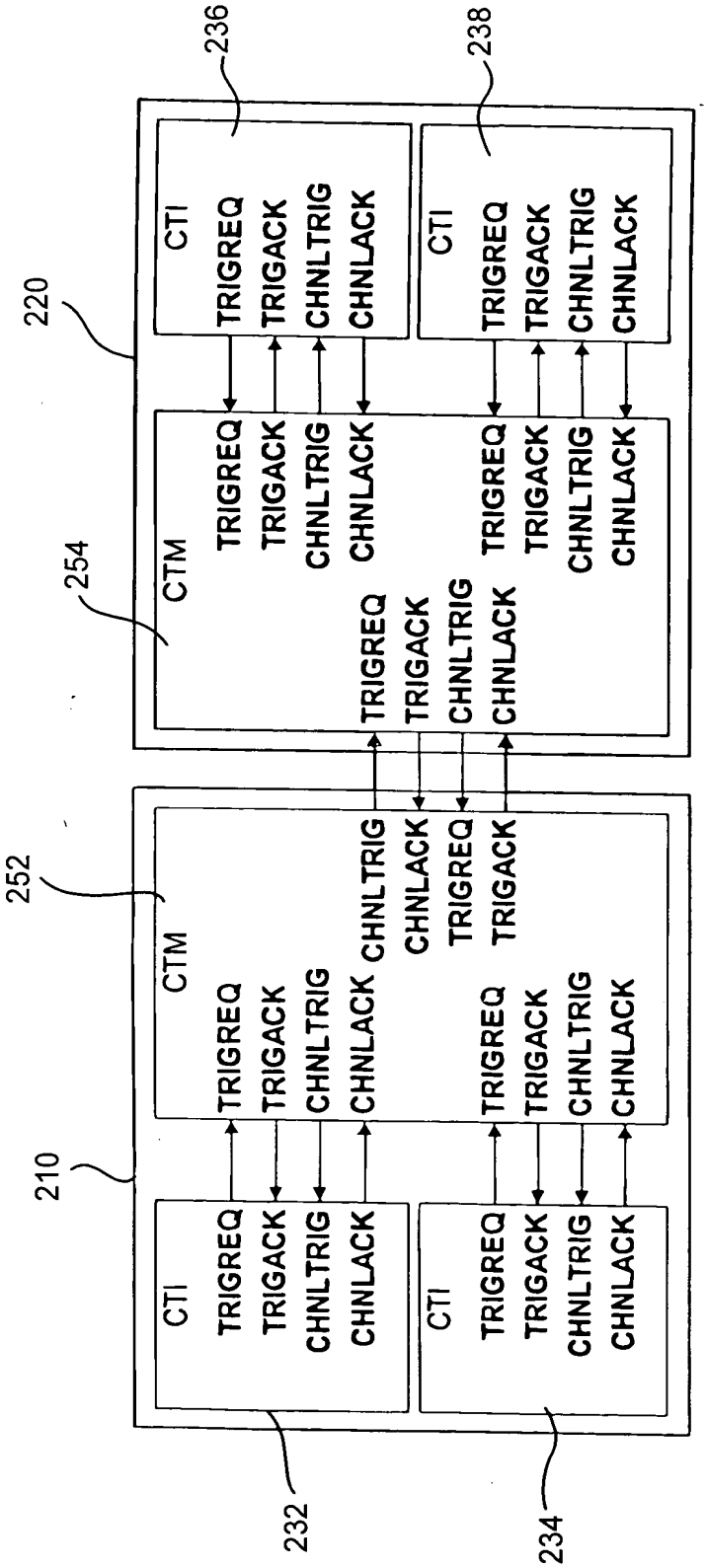
236
238
220
CTI
TRIGREQ
TRIGACK
CHNLTRIG
CHNLACK
254
CTM
252
210
232
234

FIGURE 2

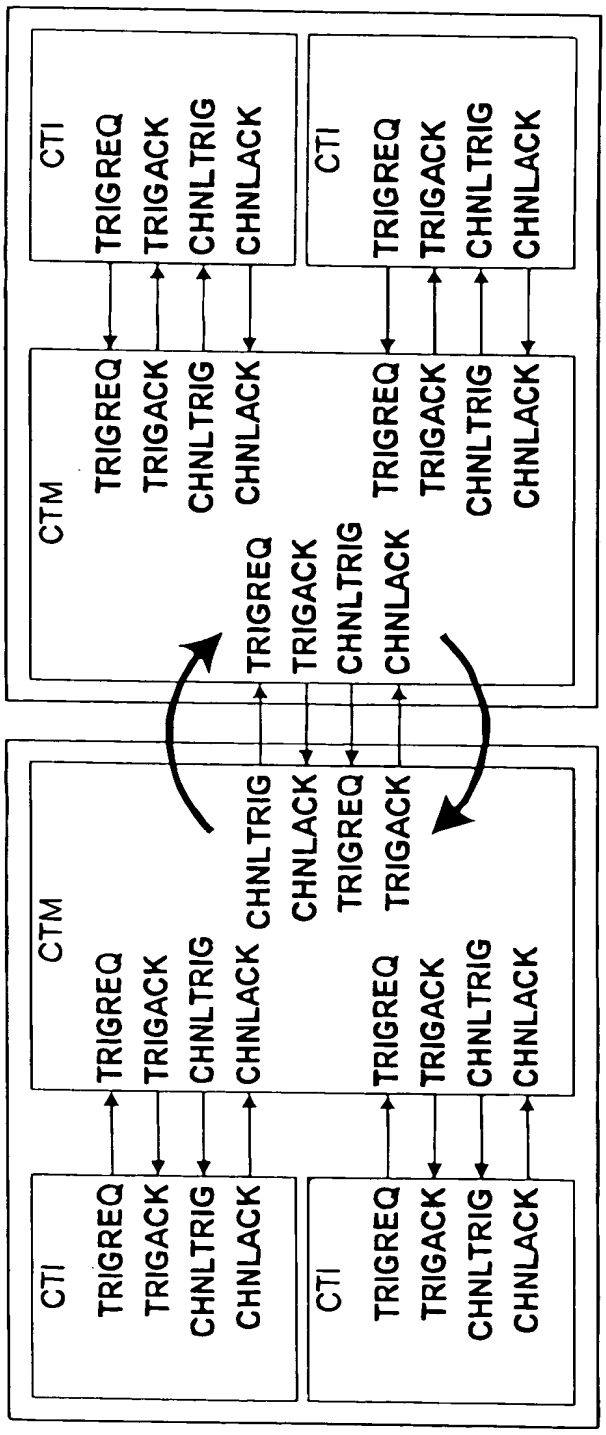
CTI
TRIGREQ
TRIGACK
CHNLTRIG
CHNLACK
CTM
TRIGREQ
TRIGACK
CHNLTRIG
CHNLACK
CHNLTRIG
CHNLACK
TRIGREQ
TRIGACK

FIGURE 3

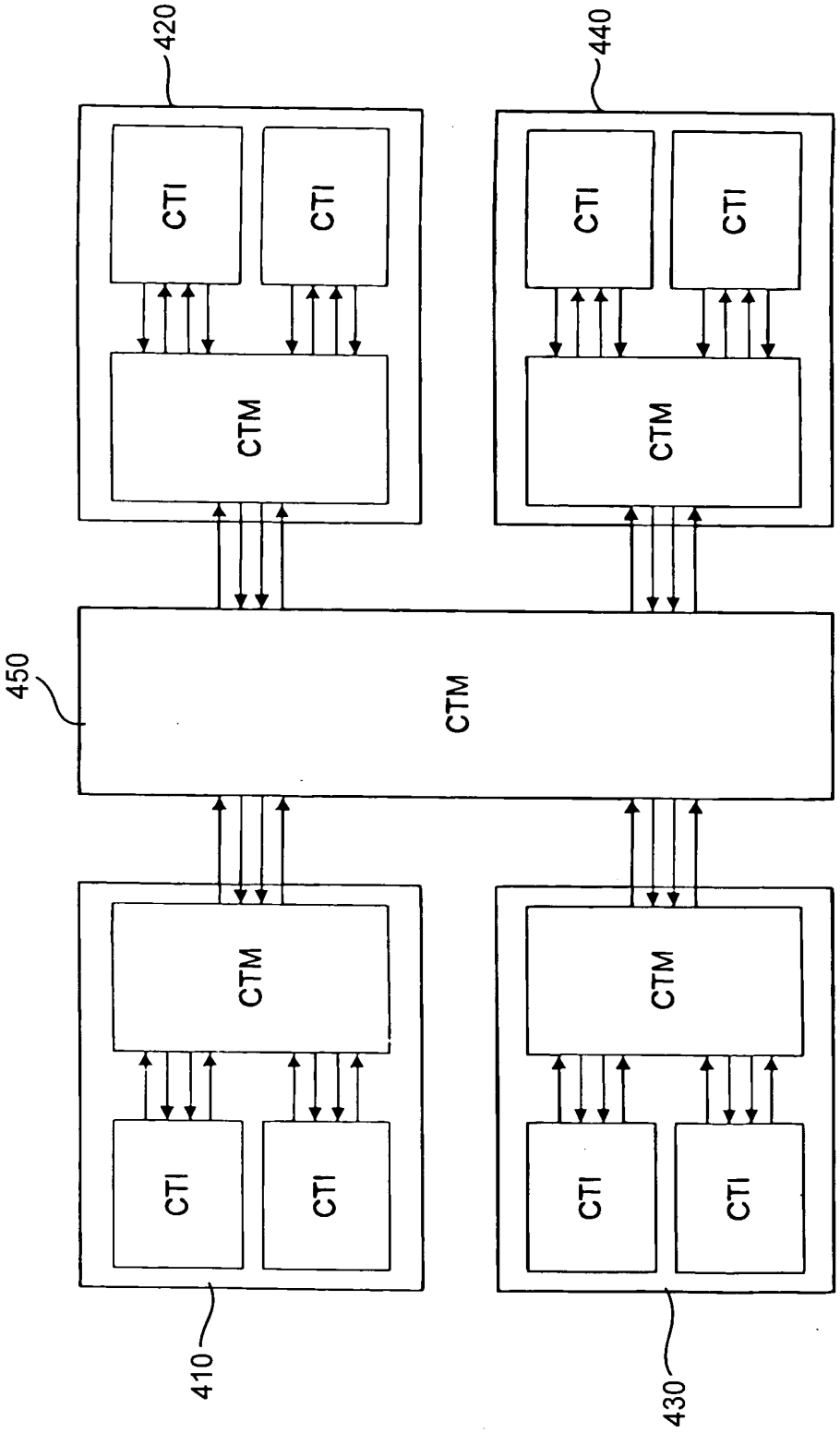
420
440
CTI
CTI
CTI
CTI
CTM
CTM
450
CTM
CTM
CTM
CTI
CTI
CTI
CTI
410
430

FIGURE 4

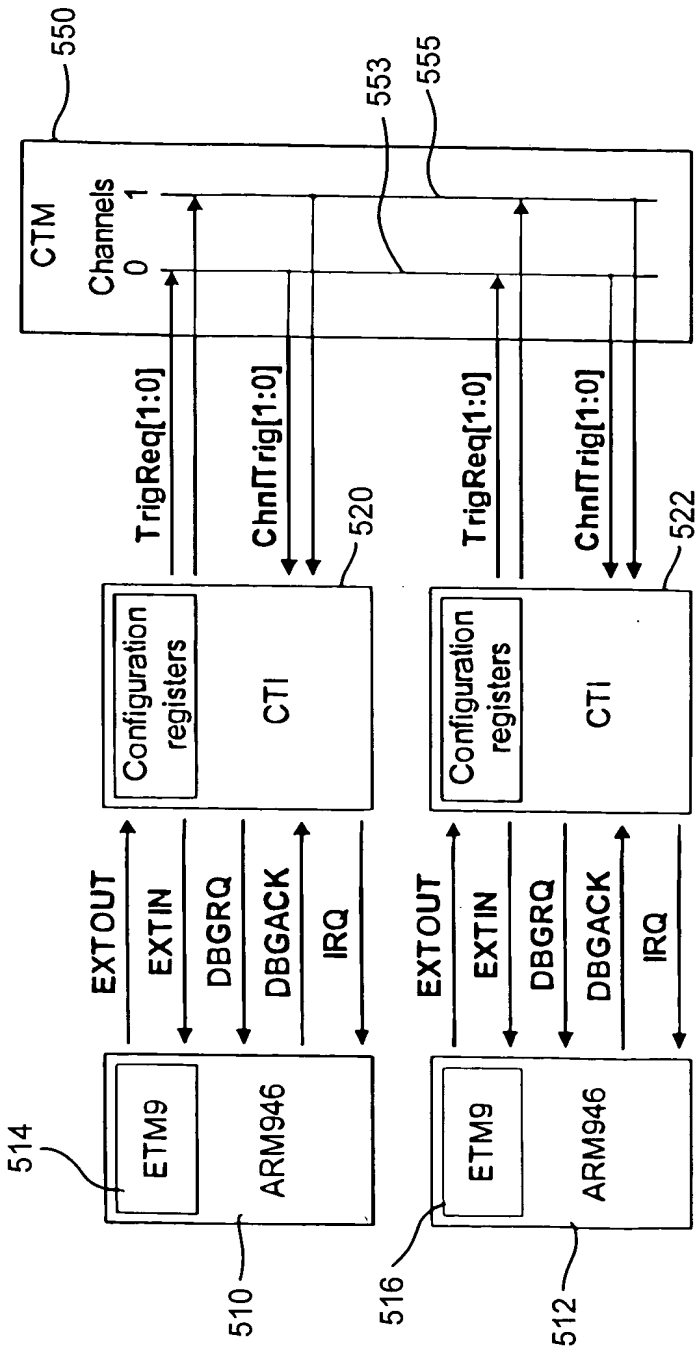
550
553
555
CTM
Channels
0
1
TrigReq[1:0]
ChnlTrig[1:0]
520
522
Configuration registers
CTI
EXTOUT
EXTIN
DBGRQ
DBGACK
IRQ
514
ETM9
ARM946
510
516
512

FIGURE 5

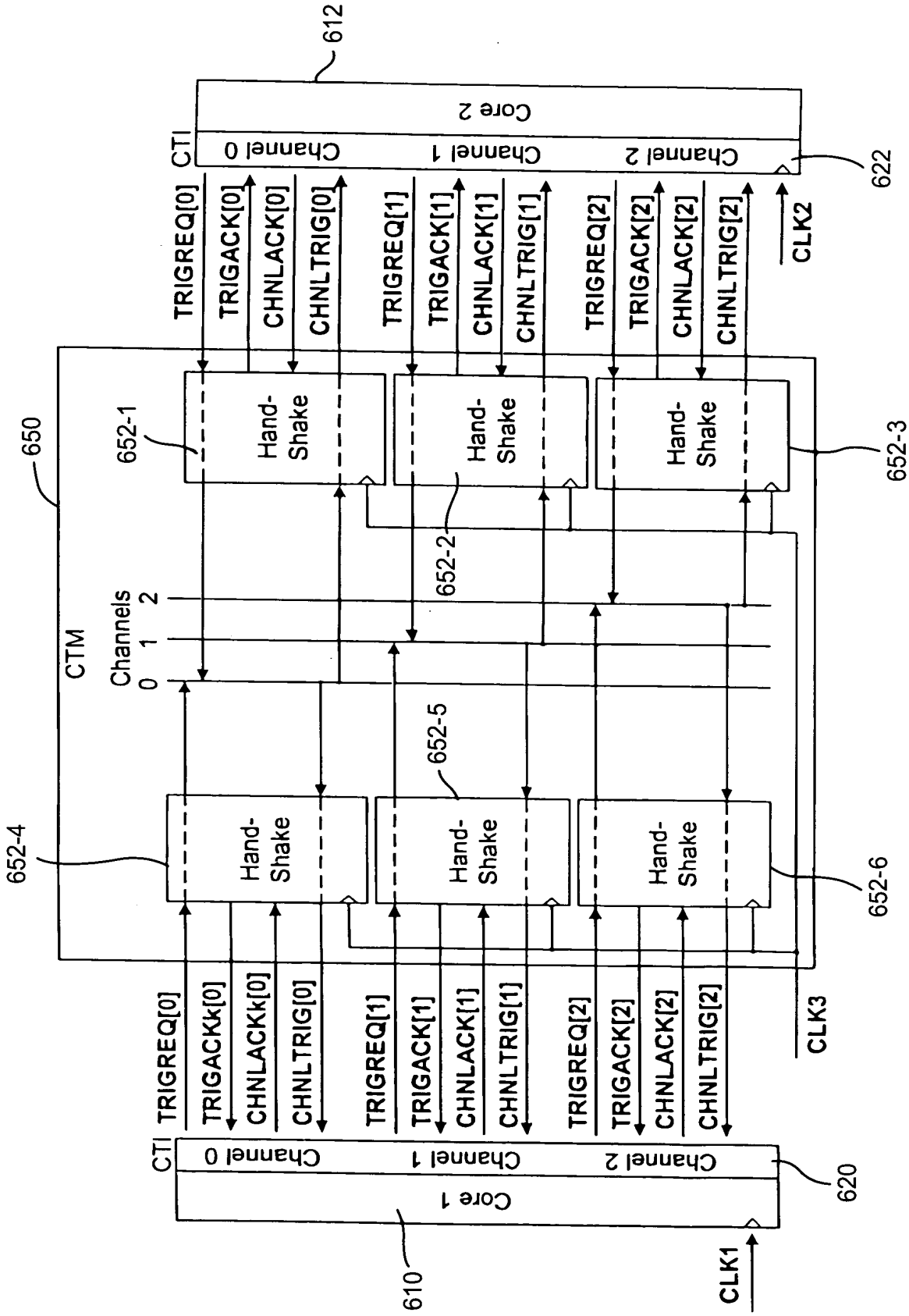
612
Core 2
CTI
Channel 0
Channel 1
Channel 2
622
TRIGREQ[0]
TRIGACK[0]
CHNLACK[0]
CHNLTRIG[0]
TRIGREQ[1]
TRIGACK[1]
CHNLACK[1]
CHNLTRIG[1]
TRIGREQ[2]
TRIGACK[2]
CHNLACK[2]
CHNLTRIG[2]
CLK2
650
652-1
Hand-Shake
652-2
652-3
CTM
Channels
0 1 2
652-4
652-5
652-6
CLK3
620
Core 1
610
CLK1

FIGURE 6

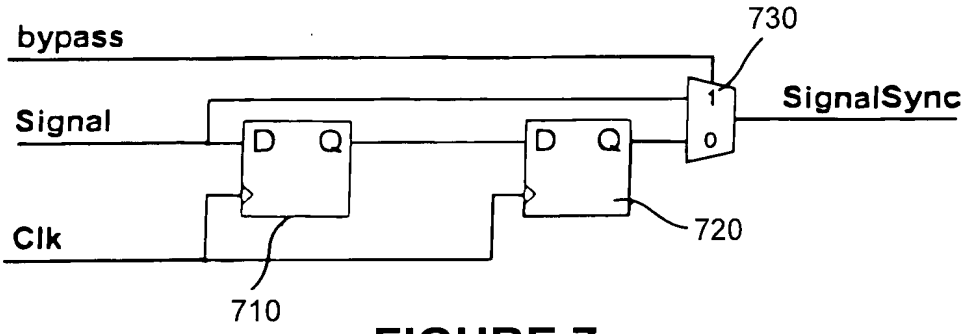

FIGURE 7

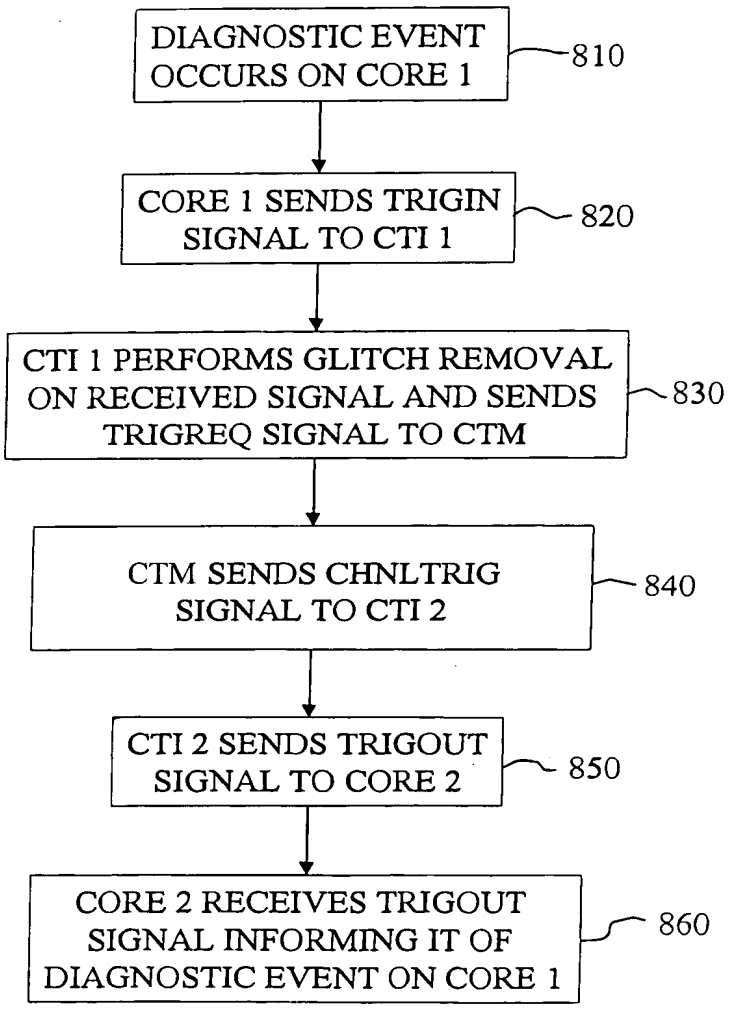

FIGURE 8

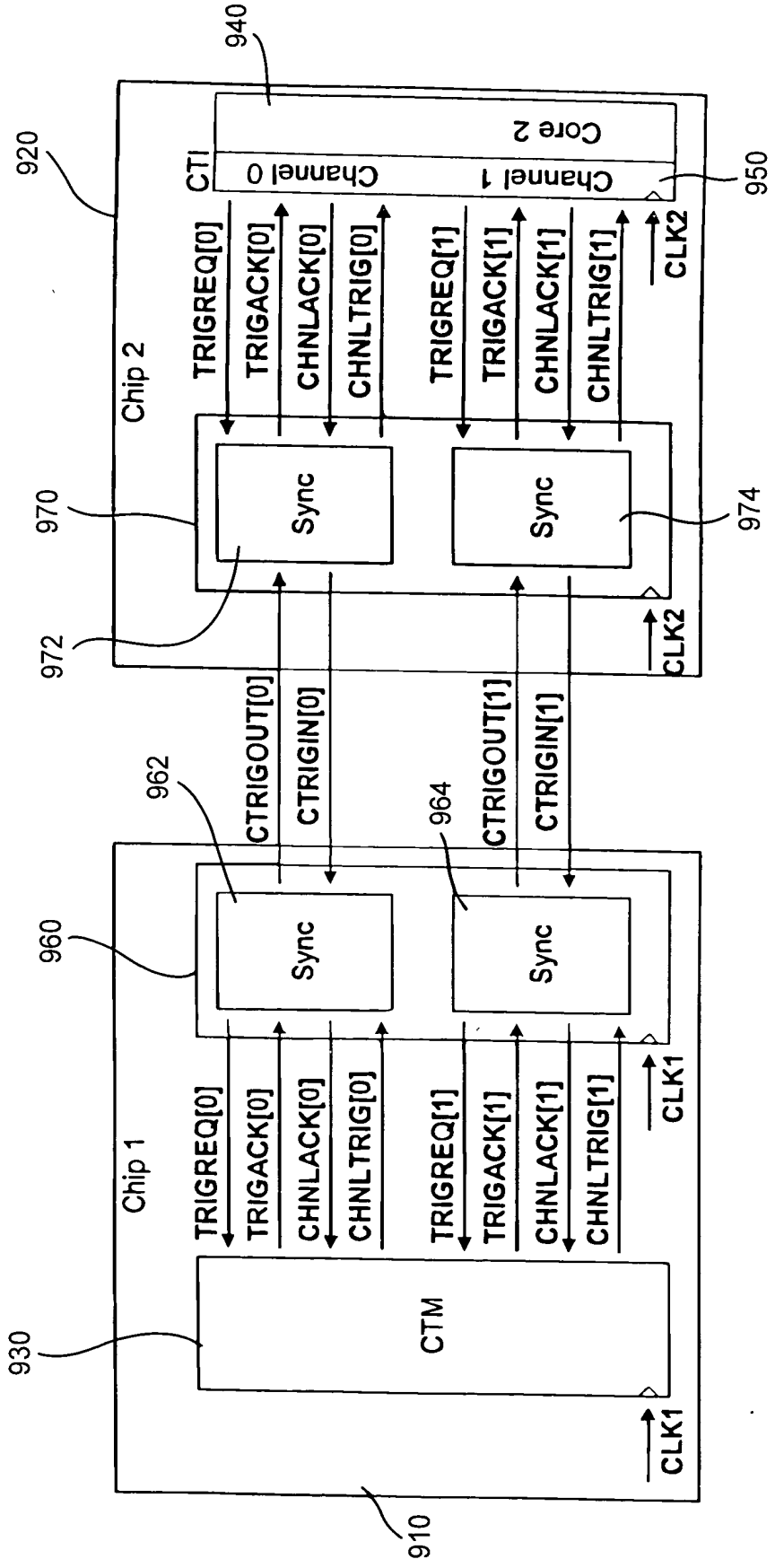
940
920
CTI
Core 2
Channel 0
Channel 1
950
TRIGREQ[0]
TRIGACK[0]
CHNLACK[0]
CHNLTRIG[0]
TRIGREQ[1]
TRIGACK[1]
CHNLACK[1]
CHNLTRIG[1]
CLK2
Chip 2
970
Sync
Sync
974
972
CLK2
CTRIGOUT[0]
CTRIGIN[0]
962
964
CTRIGOUT[1]
CTRIGIN[1]
960
Sync
Sync
TRIGREQ[0]
TRIGACK[0]
CHNLACK[0]
CHNLTRIG[0]
TRIGREQ[1]
TRIGACK[1]
CHNLACK[1]
CHNLTRIG[1]
CLK1
Chip 1
930
CTM
CLK1
910

FIGURE 9

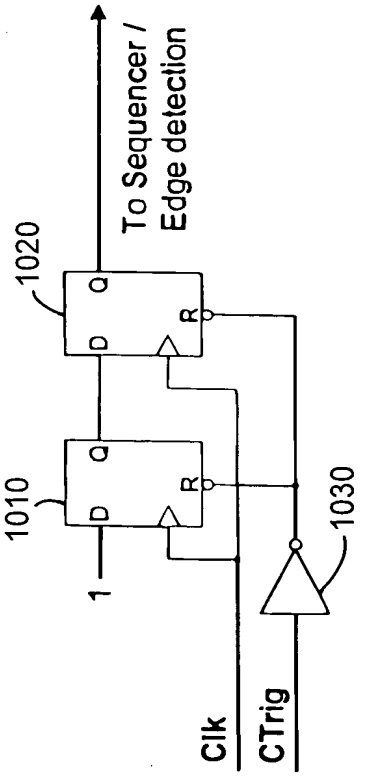

FIGURE 10

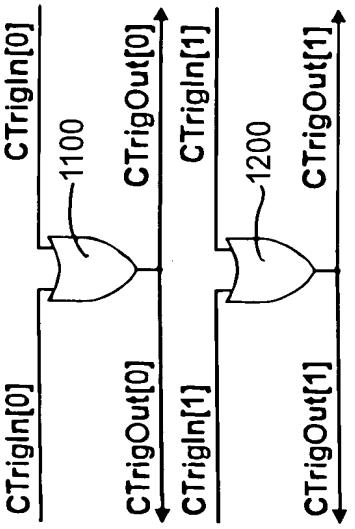

FIGURE 11B

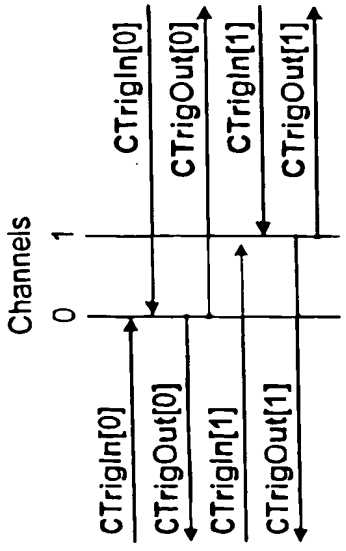

FIGURE 11A

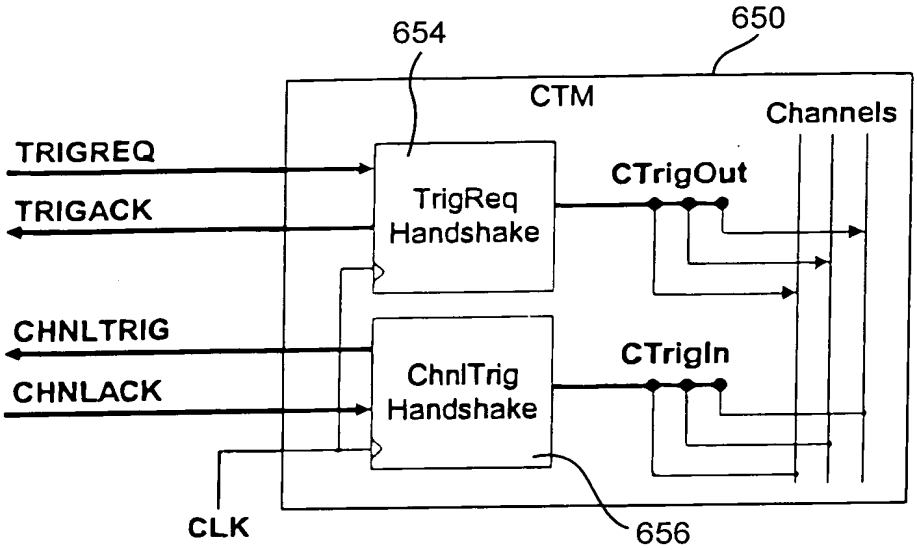

FIGURE 12

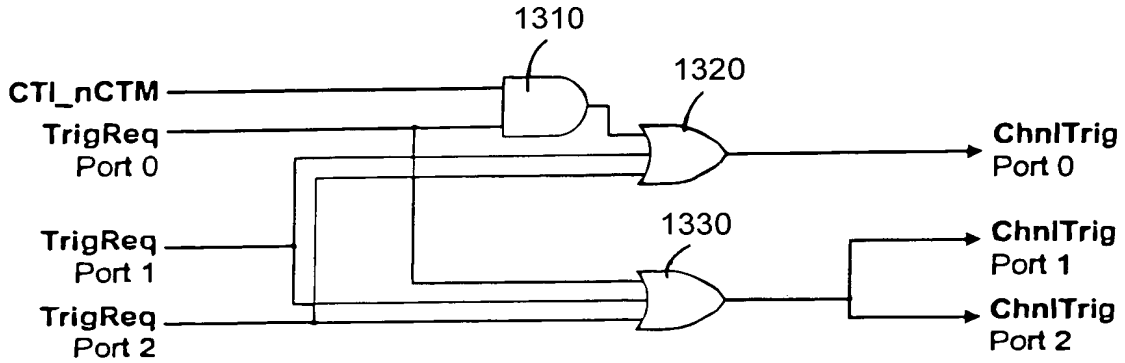

FIGURE 13

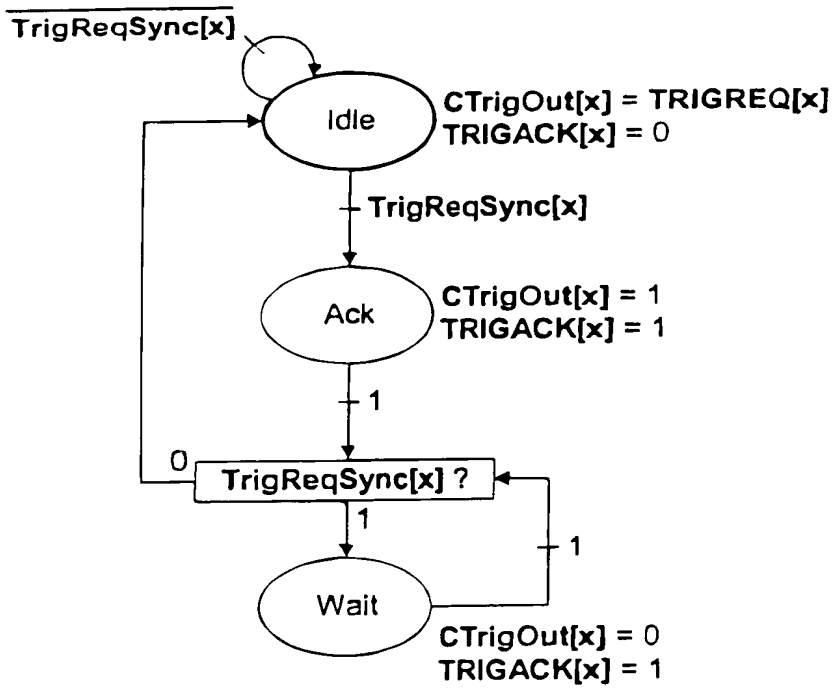

FIGURE 14

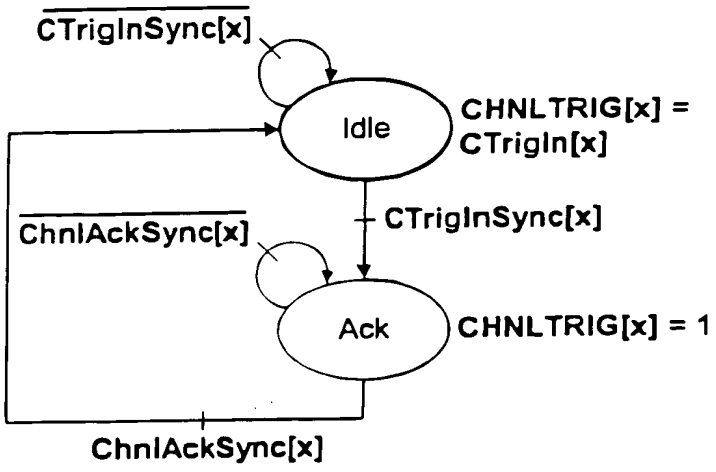

FIGURE 15

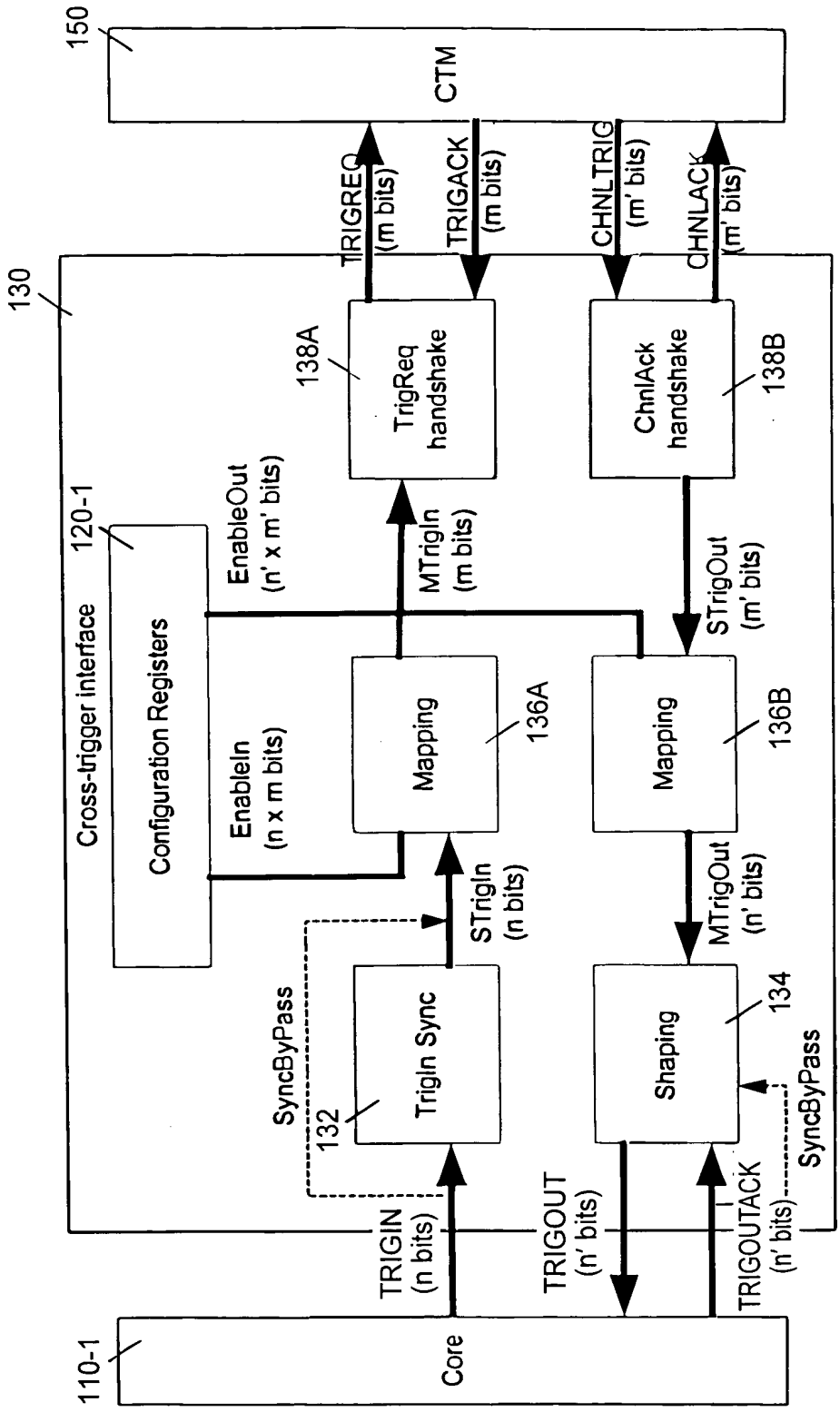
150
CTM
TRIGREQ (m bits)
TRIGACK (m bits)
CHNLTRIG (m' bits)
CHNLACK (m' bits)
130
138A
TrigReq handshake
ChnlAck handshake
138B
120-1
Cross-trigger interface
Configuration Registers
EnableOut (n' x m' bits)
MTrigIn (m bits)
STrigOut (m' bits)
EnableIn (n x m bits)
Mapping
136A
Mapping
136B
STrigIn (n bits)
MTrigOut (n' bits)
SyncByPass
132
TrigIn Sync
Shaping
134
SyncByPass
TRIGIN (n bits)
TRIGOUT (n' bits)
TRIGOUTACK (n' bits)
110-1
Core

FIGURE 16

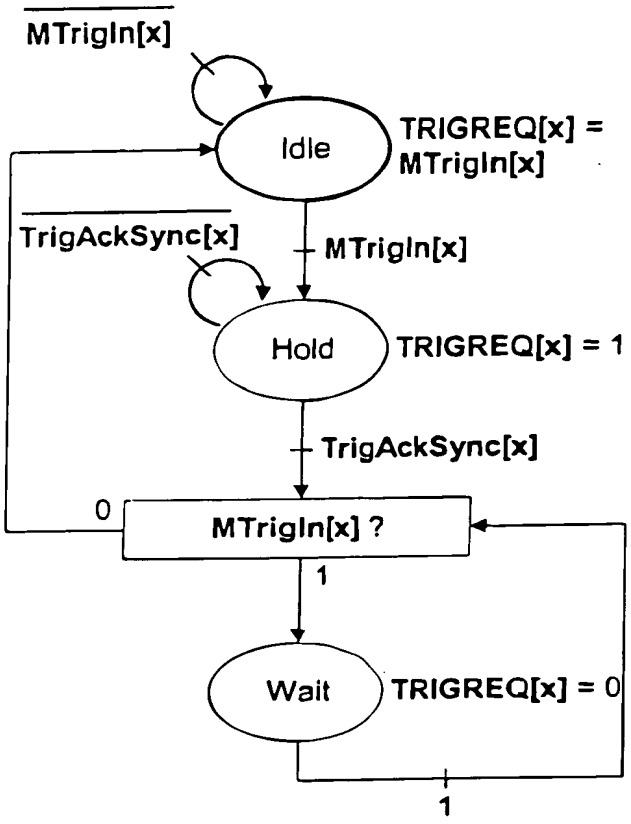

FIGURE 17

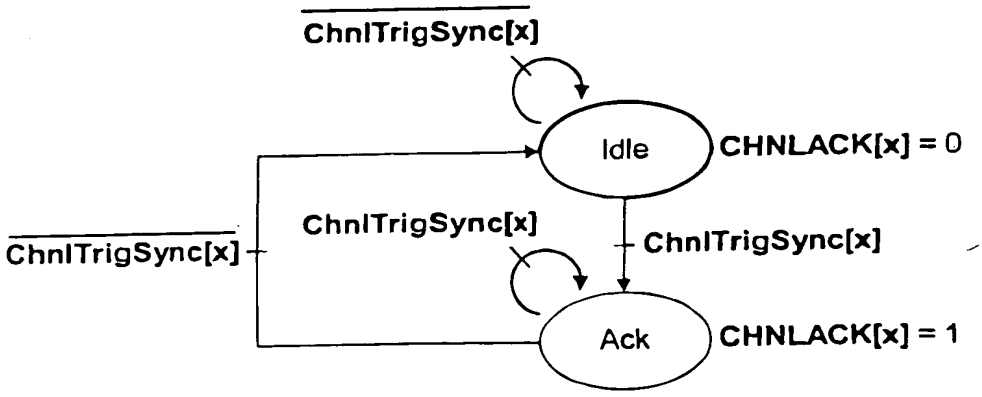

FIGURE 18

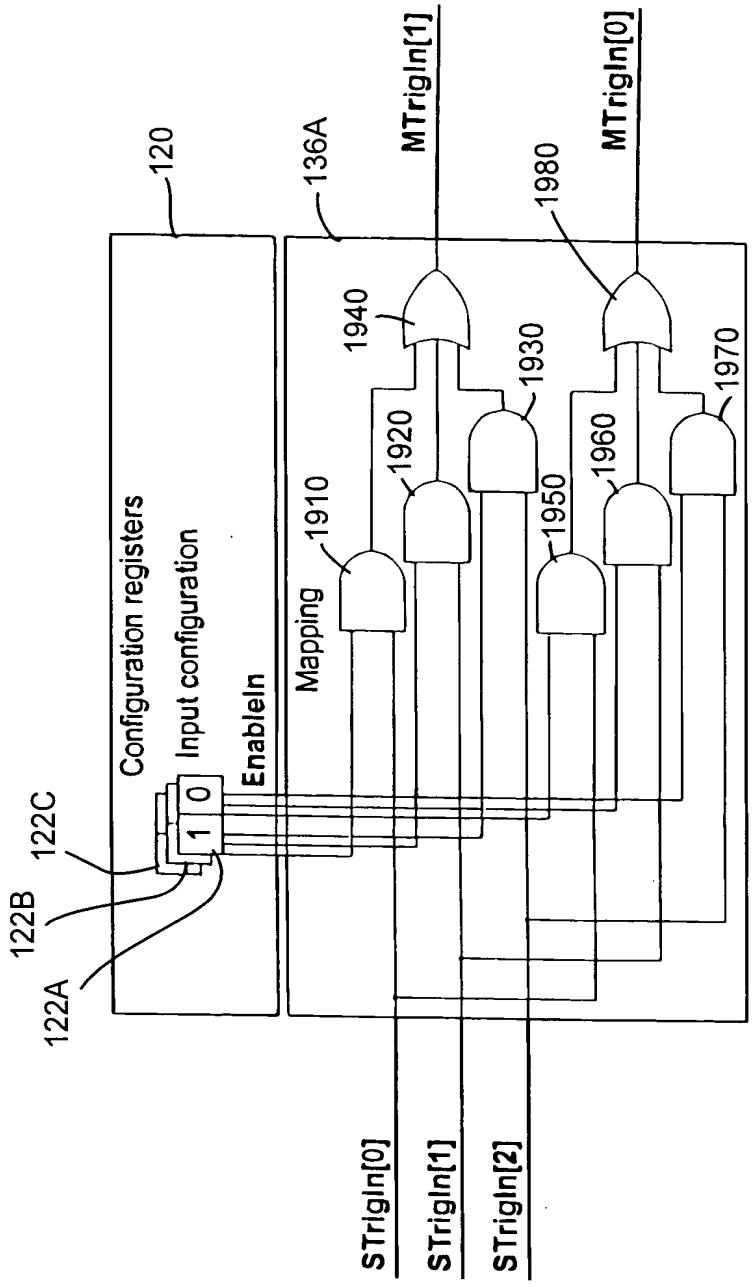
120
136A
MTrigIn[1]
MTrigIn[0]
1980
1940
1930
1970
1920
1960
1910
1950
Configuration registers
Input configuration
EnableIn
Mapping
122C
122B
122A
1
0
STrigIn[0]
STrigIn[1]
STrigIn[2]

FIGURE 19

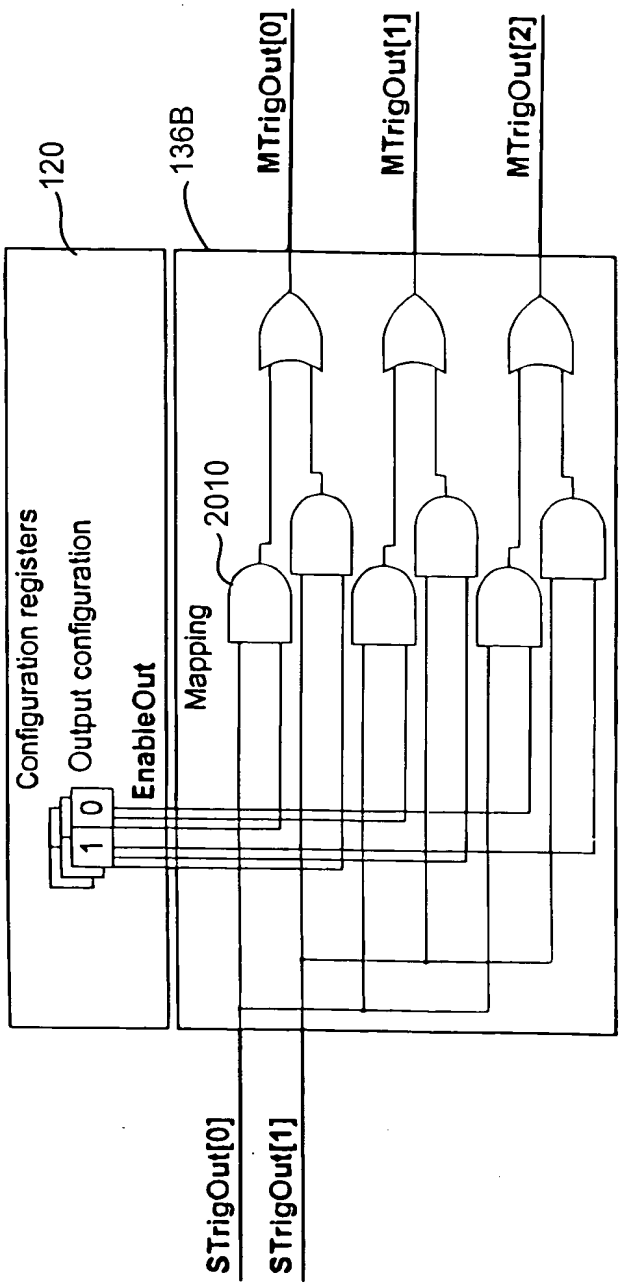
120
136B
MTrigOut[0]
MTrigOut[1]
MTrigOut[2]
Configuration registers
Output configuration
EnableOut
Mapping
2010
1
0
STrigOut[0]
STrigOut[1]

FIGURE 20

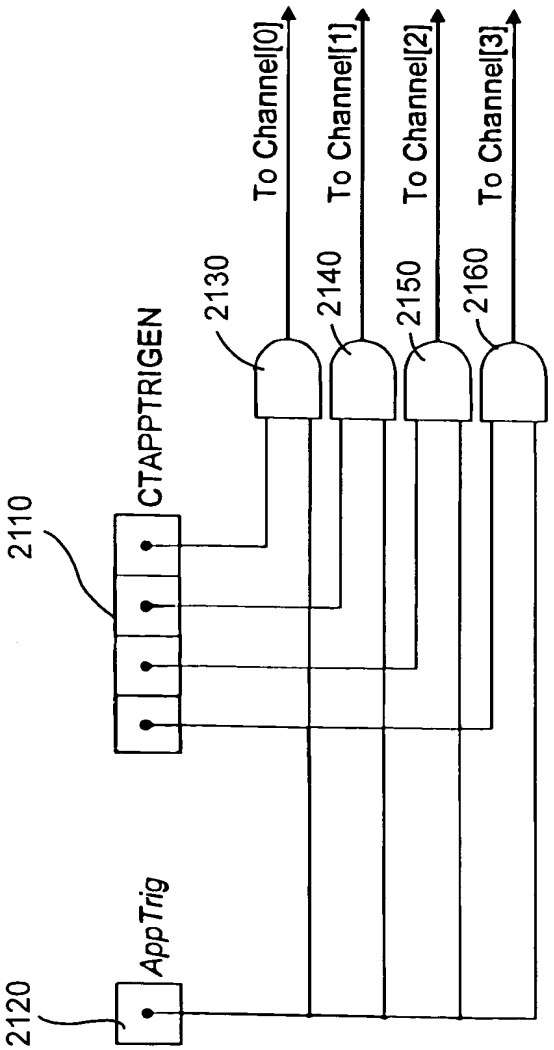
To Channel[0]
To Channel[1]
To Channel[2]
To Channel[3]
2130
2140
2150
2160
CTAPPTRIGEN
2110
AppTrig
2120

FIGURE 21

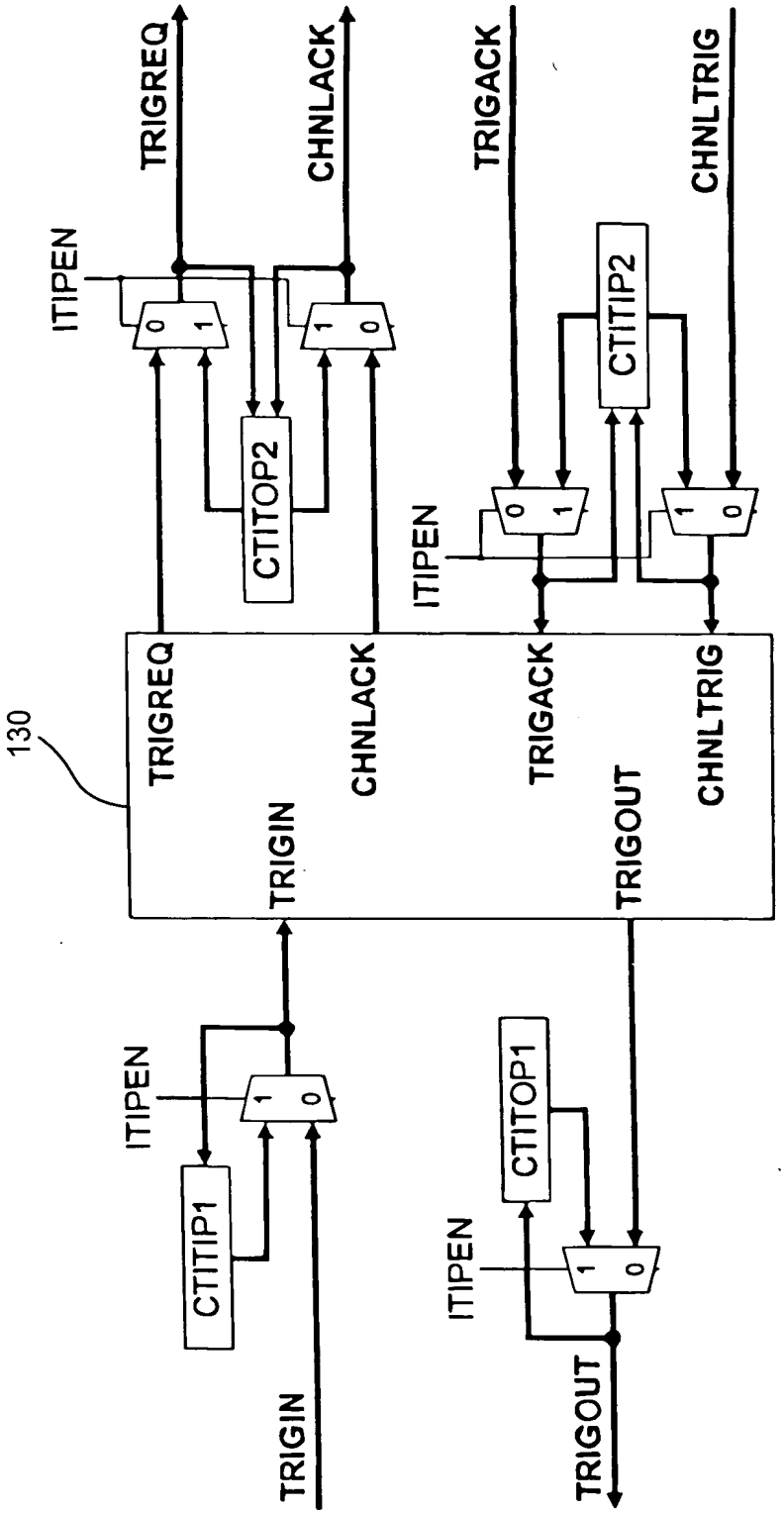
130
TRIGREQ
CHNLACK
TRIGACK
CHNLTRIG
TRIGIN
TRIGOUT
ITIPEN
CTITOP2
CTITIP2
CTITIP1
CTITOP1
0
1

FIGURE 22

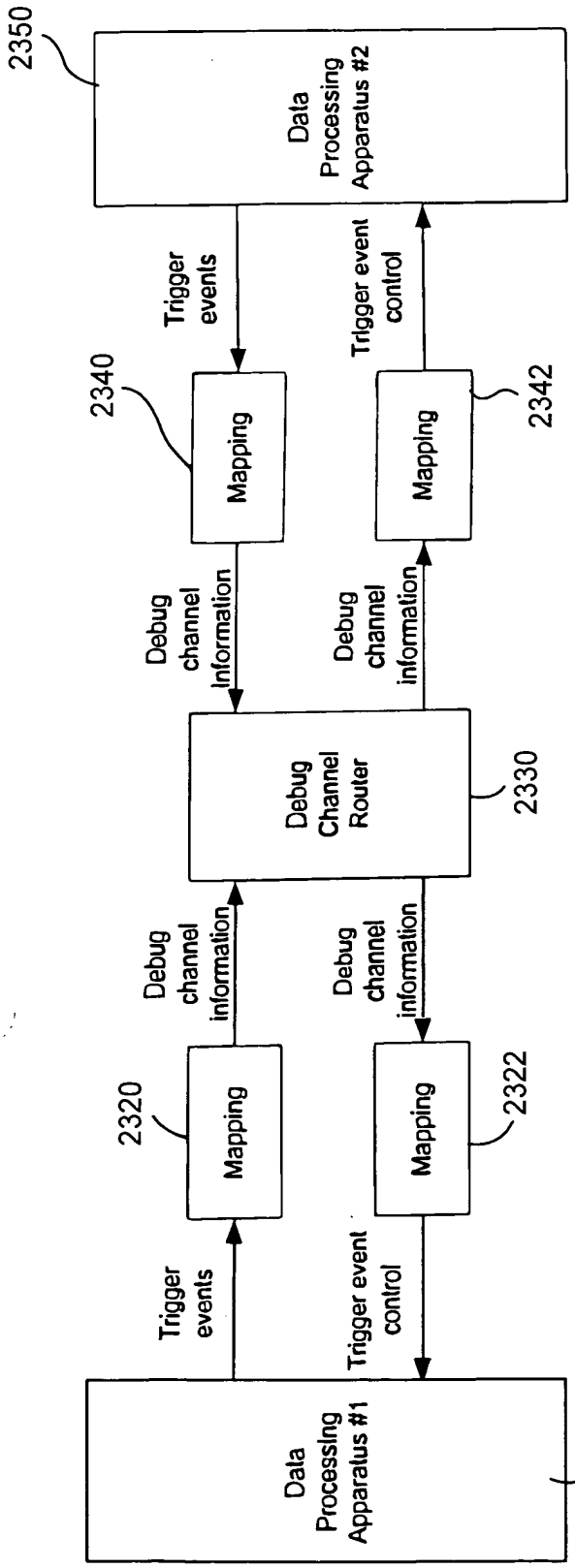
2350
Data Processing Apparatus #2
Trigger events
Trigger event control
2340
Mapping
2342
Mapping
Debug channel information
Debug channel information
Debug Channel Router
2330
Debug channel information
Debug channel information
2320
Mapping
2322
Mapping
Trigger events
Trigger event control
Data Processing Apparatus #1
2310

FIGURE 23

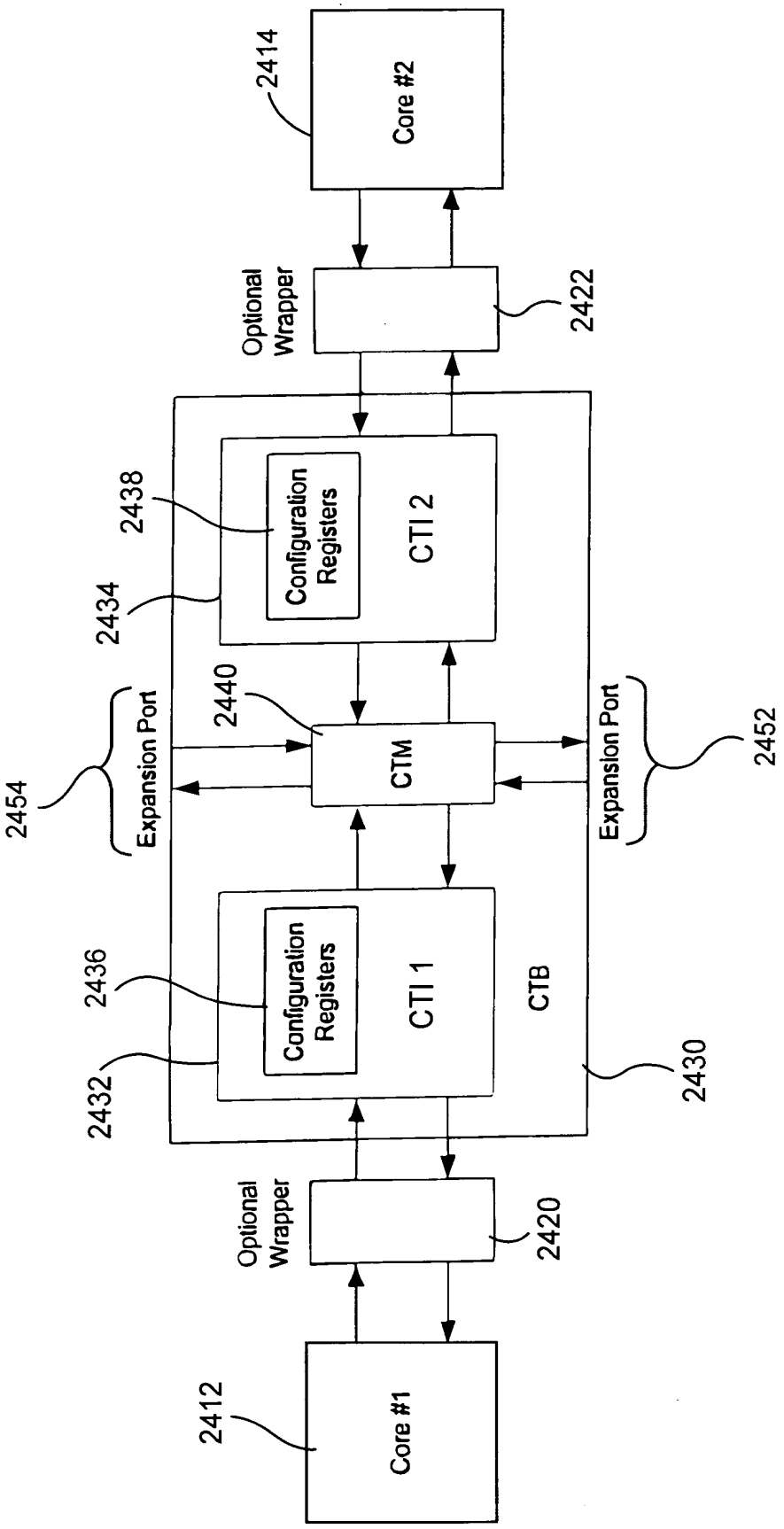
2414
Core #2
Optional Wrapper
2422
2438
Configuration Registers
CTI 2
2434
2440
CTM
2454
Expansion Port
Expansion Port
2452
2436
Configuration Registers
CTI 1
CTB
2432
2430
Optional Wrapper
2420
2412
Core #1

FIGURE 24

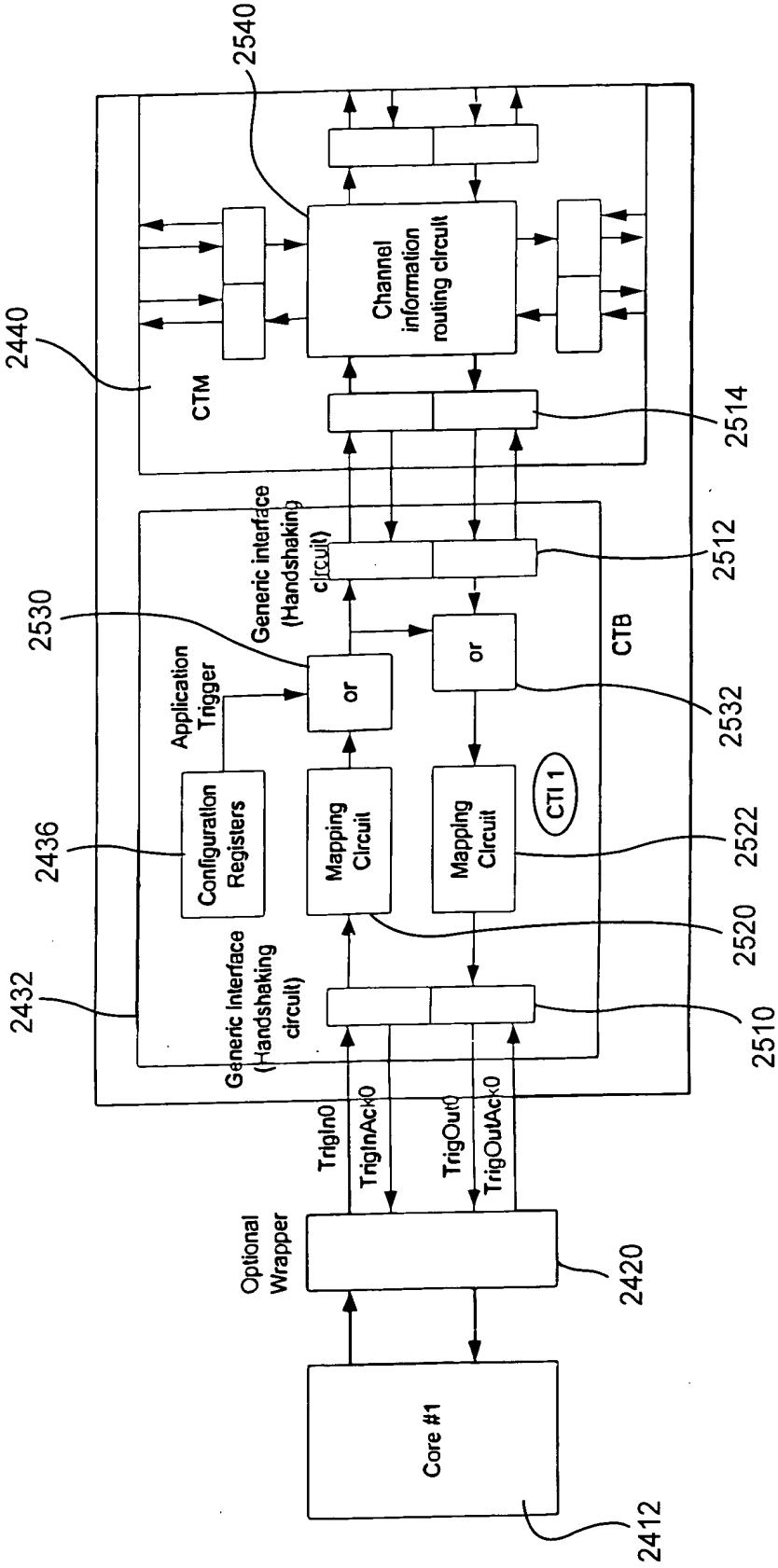
2540
Channel information routing circuit
2440
CTM
2514
2512
Generic interface (Handshaking circuit)
2530
Application Trigger
or
or
CTB
2532
2436
Configuration Registers
Mapping Circuit
Mapping Circuit
CTI 1
2522
2520
2432
Generic Interface (Handshaking circuit)
2510
TrigIn0
TrigInAck0
TrigOut0
TrigOutAck0
Optional Wrapper
2420
Core #1
2412

FIGURE 25

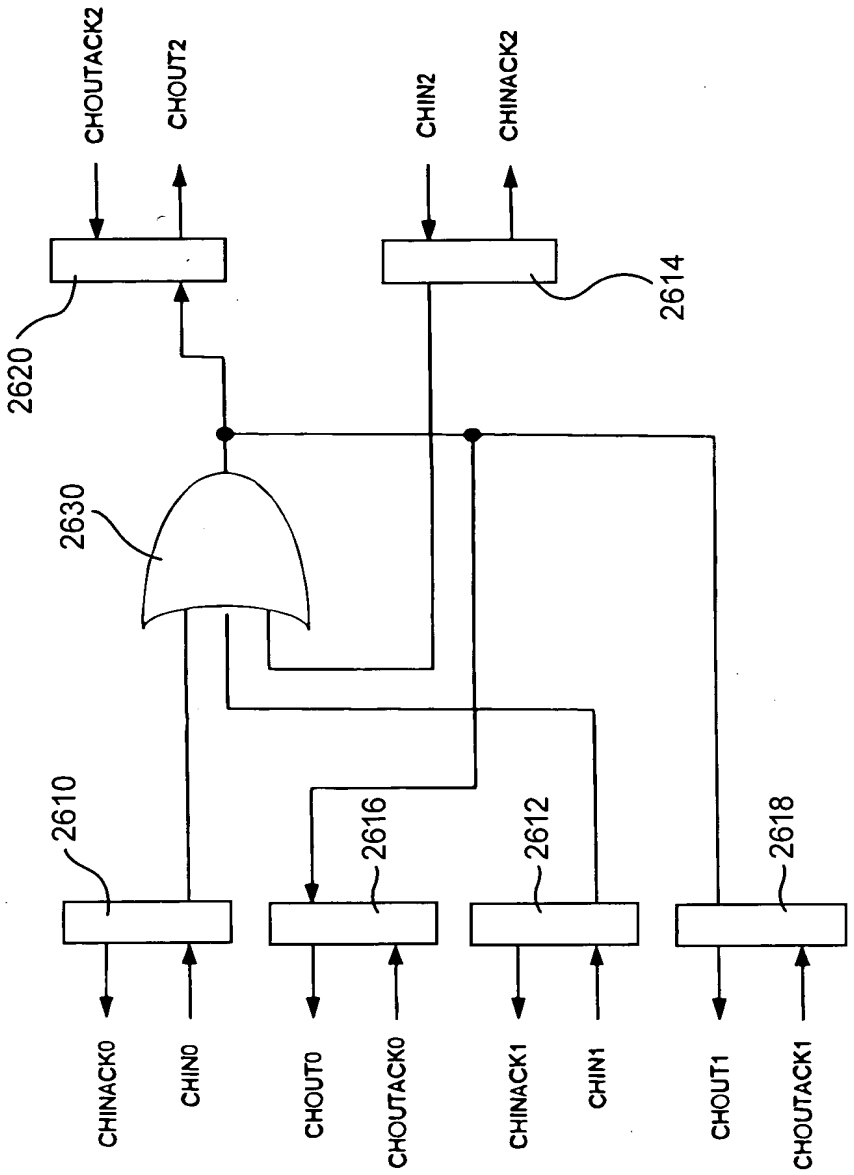
CHOUTACK2
CHOUT2
CHIN2
CHINACK2
2620
2614
2630
2610
2616
2612
2618
CHINACK0
CHIN0
CHOUT0
CHOUTACK0
CHINACK1
CHIN1
CHOUT1
CHOUTACK1

FIGURE 26

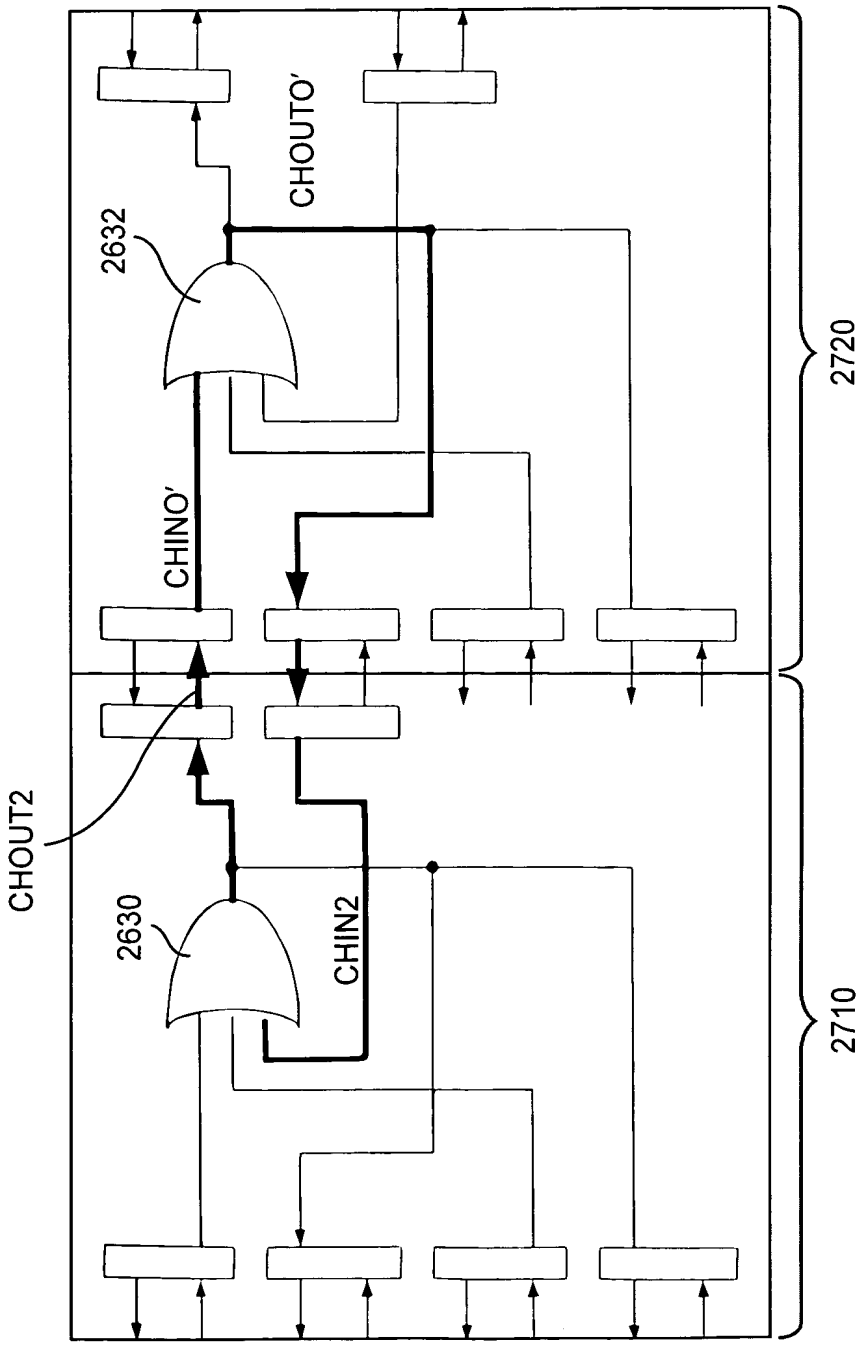

FIGURE 27

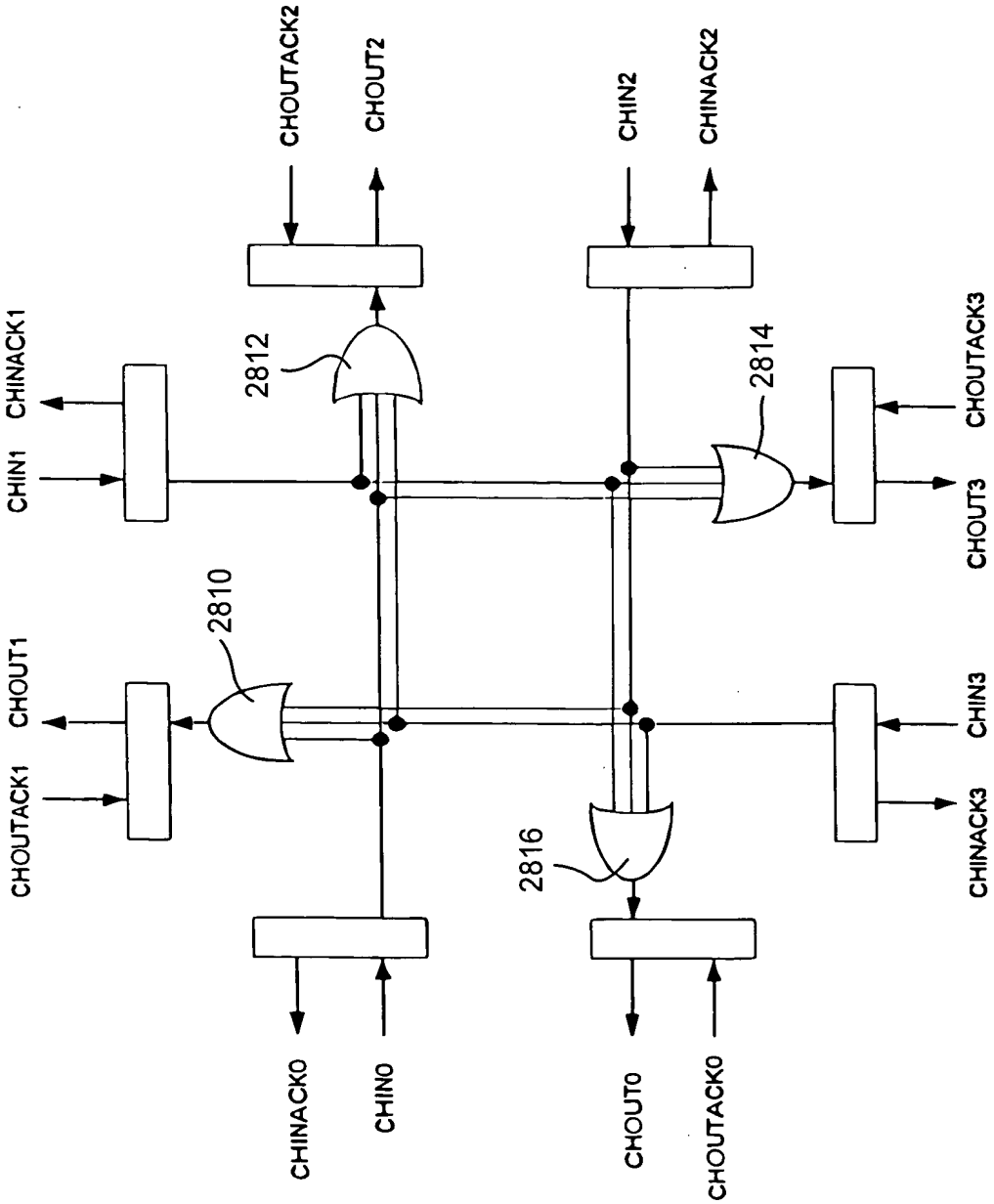
CHOUTACK2
CHOUT2
CHIN2
CHINACK2
CHINACK1
CHIN1
2812
2814
CHOUTACK3
CHOUT3
2810
CHOUT1
CHOUTACK1
CHIN3
CHINACK3
2816
CHINACK0
CHIN0
CHOUT0
CHOUTACK0

FIGURE 28

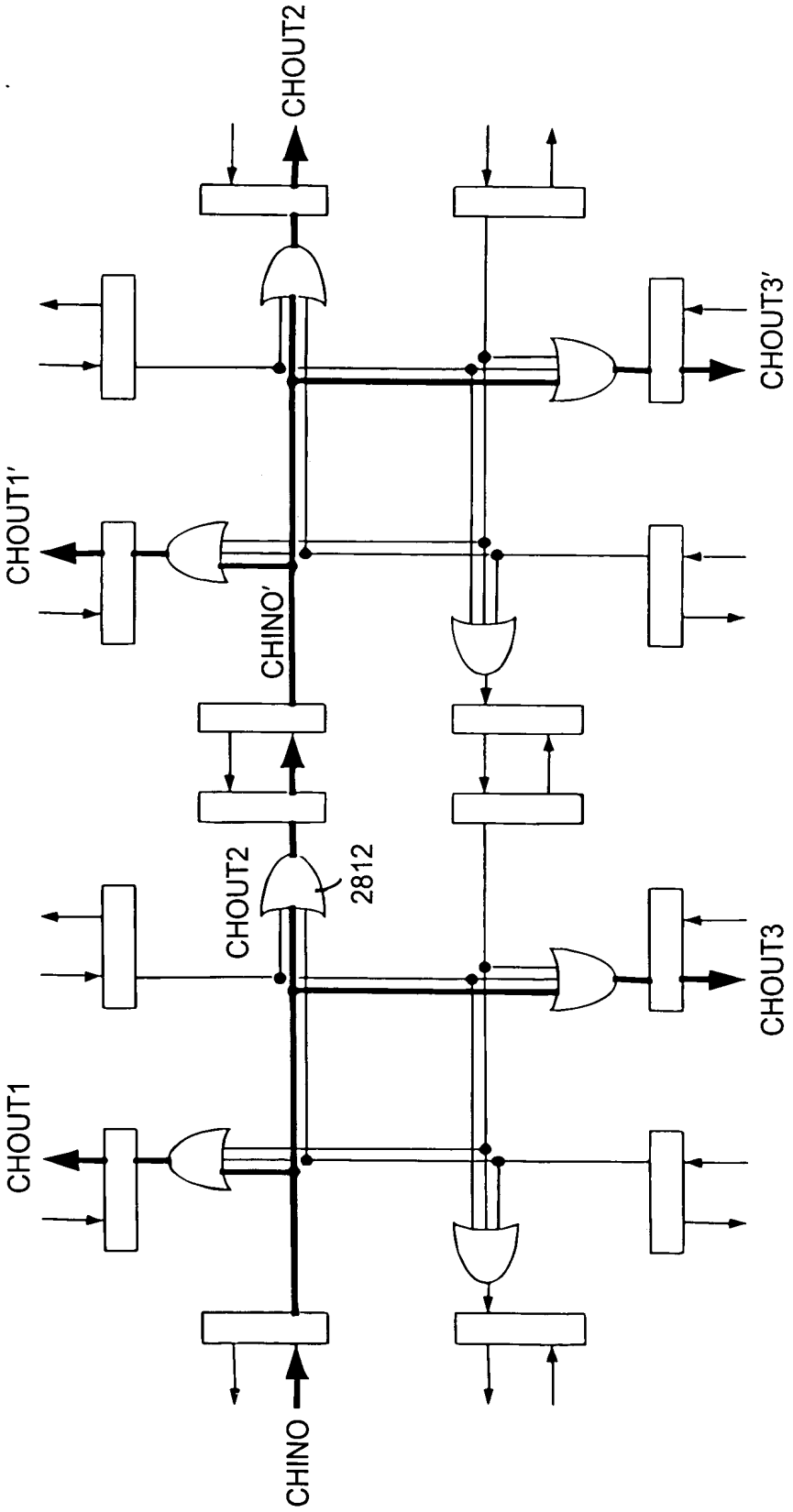
CHOUT2
CHOUT3'
CHOUT1'
CHINO'
CHOUT2
2812
CHOUT3
CHOUT1
CHINO

FIGURE 29

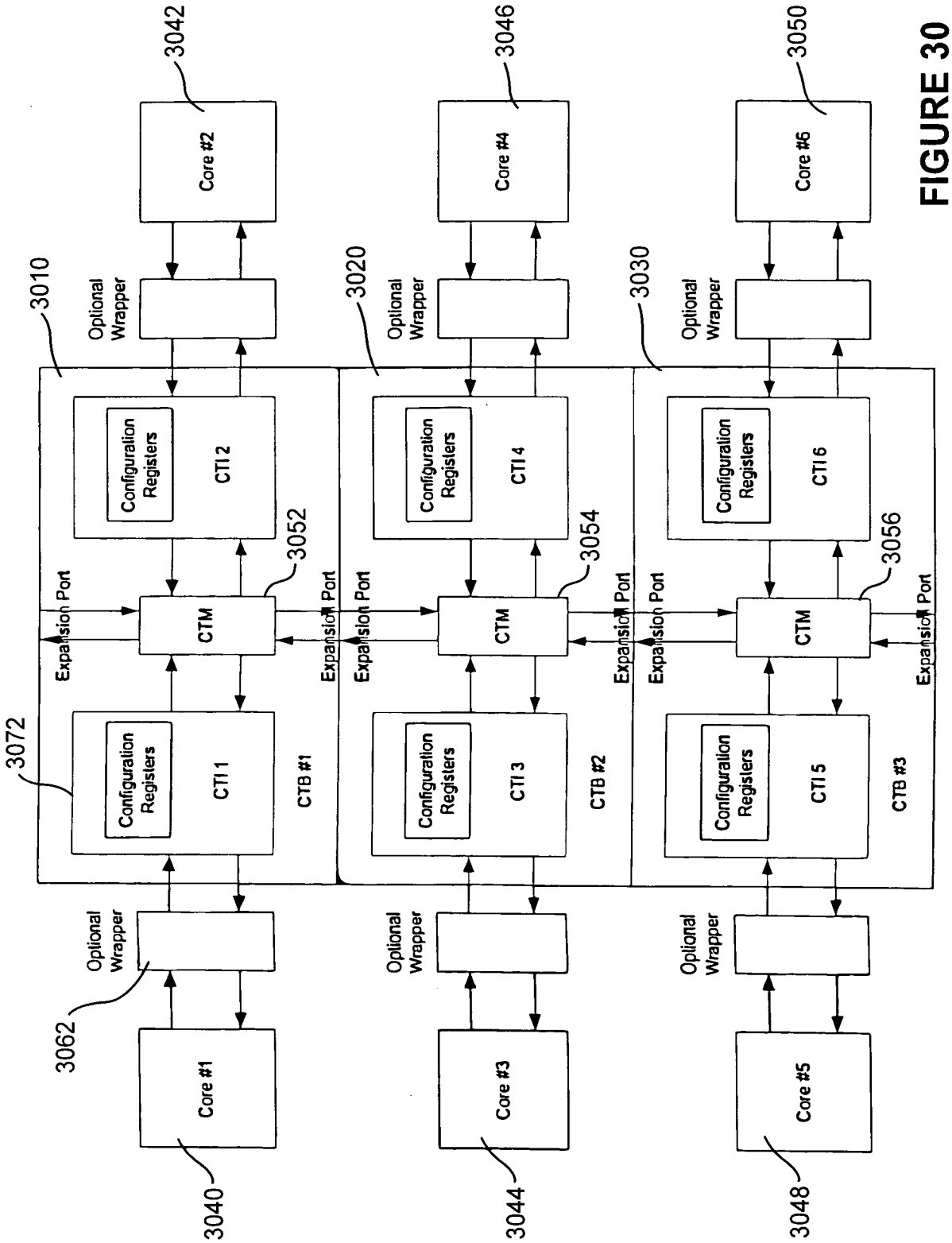
3042
Core #2
3046
Core #4
3050
Core #6
3010
3020
3030
Optional Wrapper
Configuration Registers
CTI 2
CTI 4
CTI 6
3052
3054
3056
Expansion Port
CTM
3072
CTI 1
CTI 3
CTI 5
CTB #1
CTB #2
CTB #3
3062
Core #1
Core #3
Core #5
3040
3044
3048

FIGURE 30

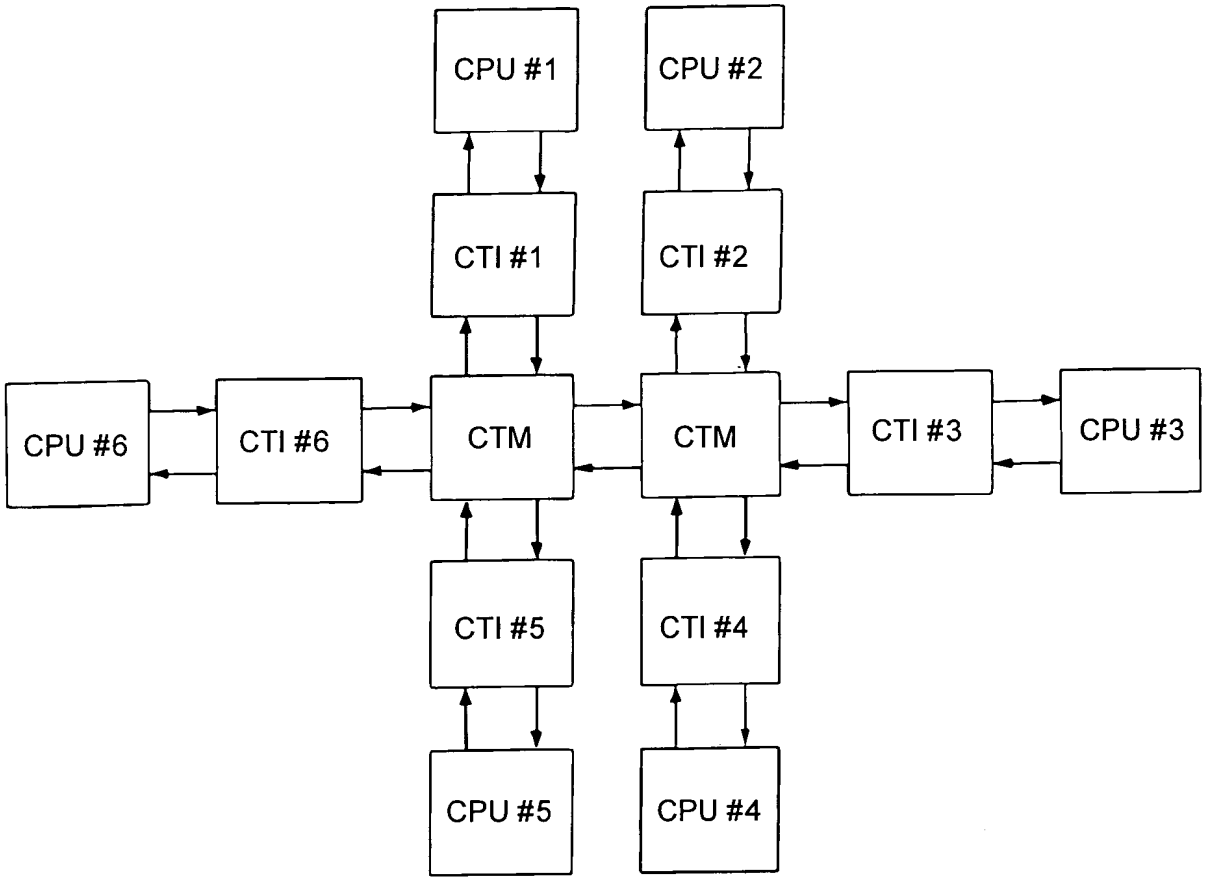

FIGURE 31

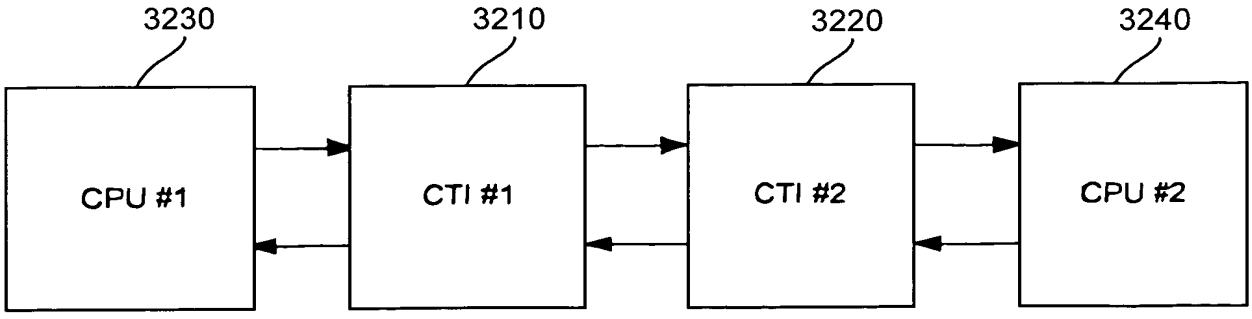

FIGURE 32

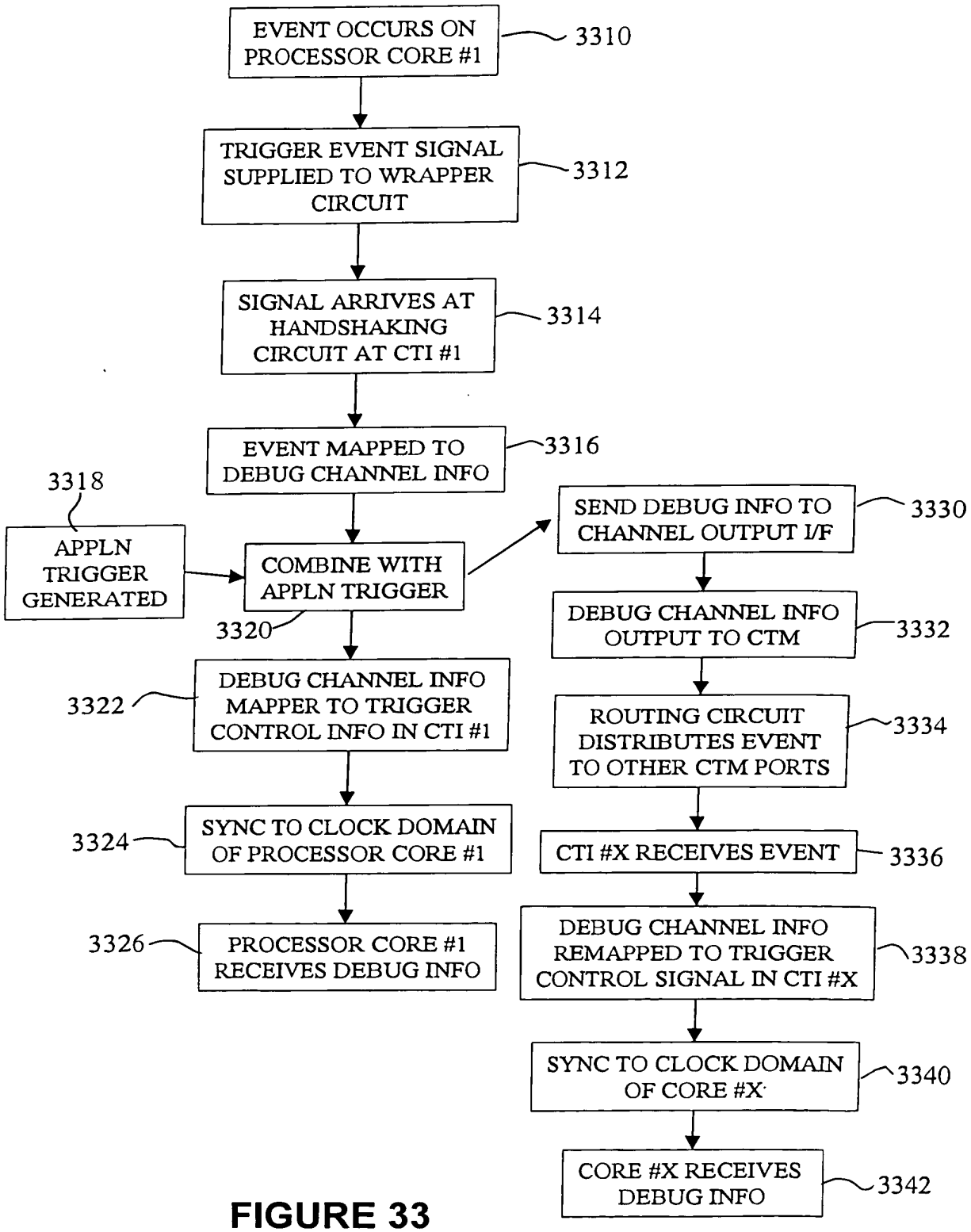
EVENT OCCURS ON PROCESSOR CORE #1
3310
TRIGGER EVENT SIGNAL SUPPLIED TO WRAPPER CIRCUIT
3312
SIGNAL ARRIVES AT HANDSHAKING CIRCUIT AT CTI #1
3314
EVENT MAPPED TO DEBUG CHANNEL INFO
3316
3318
APPLN TRIGGER GENERATED
COMBINE WITH APPLN TRIGGER
3320
SEND DEBUG INFO TO CHANNEL OUTPUT I/F
3330
DEBUG CHANNEL INFO OUTPUT TO CTM
3332
3322
DEBUG CHANNEL INFO MAPPER TO TRIGGER CONTROL INFO IN CTI #1
ROUTING CIRCUIT DISTRIBUTES EVENT TO OTHER CTM PORTS
3334
3324
SYNC TO CLOCK DOMAIN OF PROCESSOR CORE #1
CTI #X RECEIVES EVENT
3336
3326
PROCESSOR CORE #1 RECEIVES DEBUG INFO
DEBUG CHANNEL INFO REMAPPED TO TRIGGER CONTROL SIGNAL IN CTI #X
3338
SYNC TO CLOCK DOMAIN OF CORE #X
3340
CORE #X RECEIVES DEBUG INFO
3342

FIGURE 33

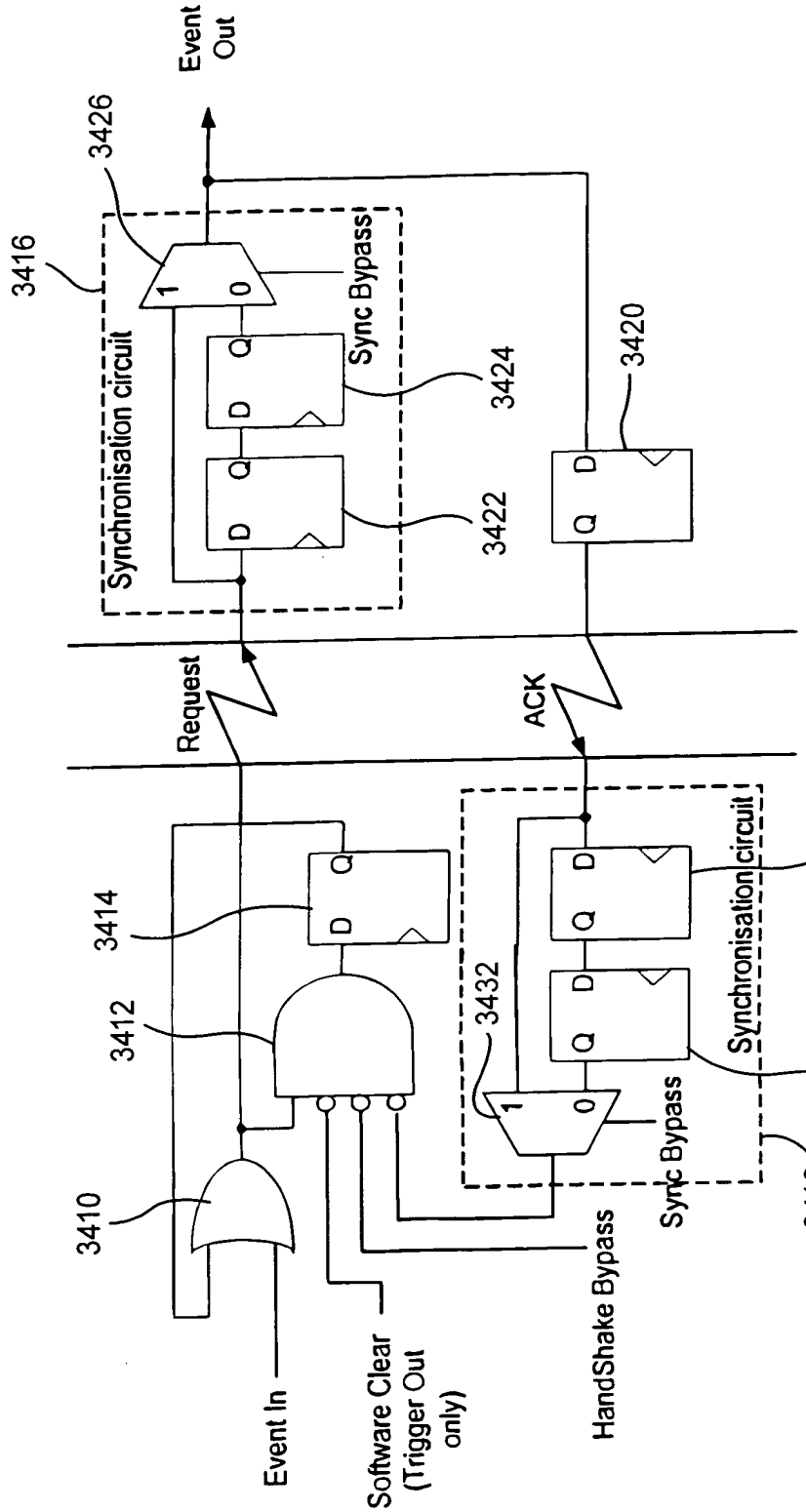
Event Out
3426
3416
Synchronisation circuit
Sync Bypass
3424
3422
3420
Request
ACK
3414
3412
3410
3432
3430
Synchronisation circuit
3428
3418
Sync Bypass
HandShake Bypass
Event In
Software Clear (Trigger Out only)

FIGURE 34

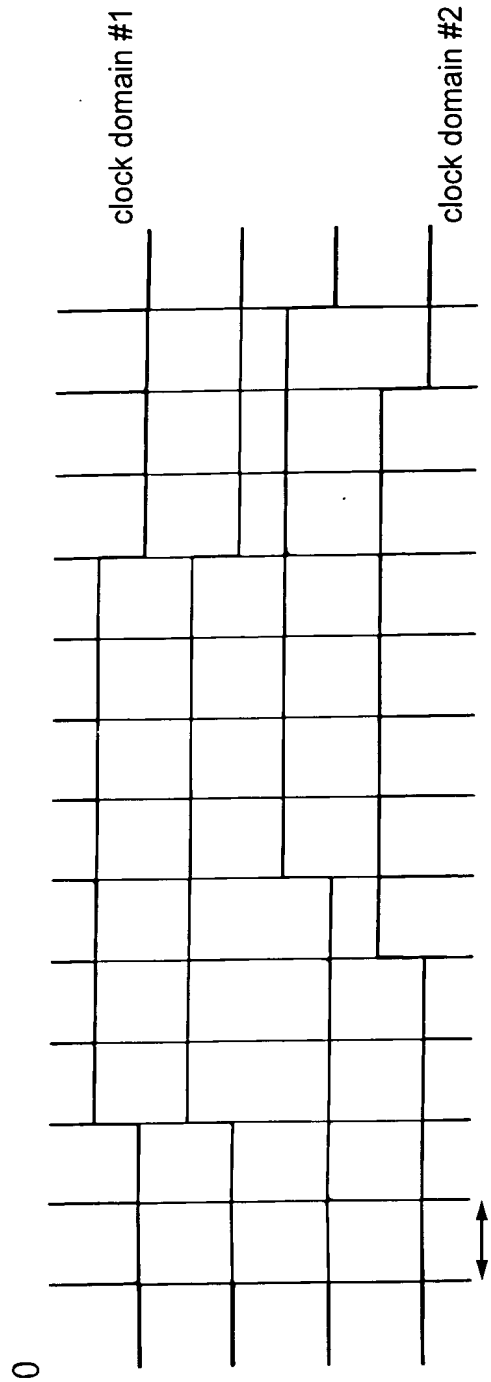

FIGURE 35A

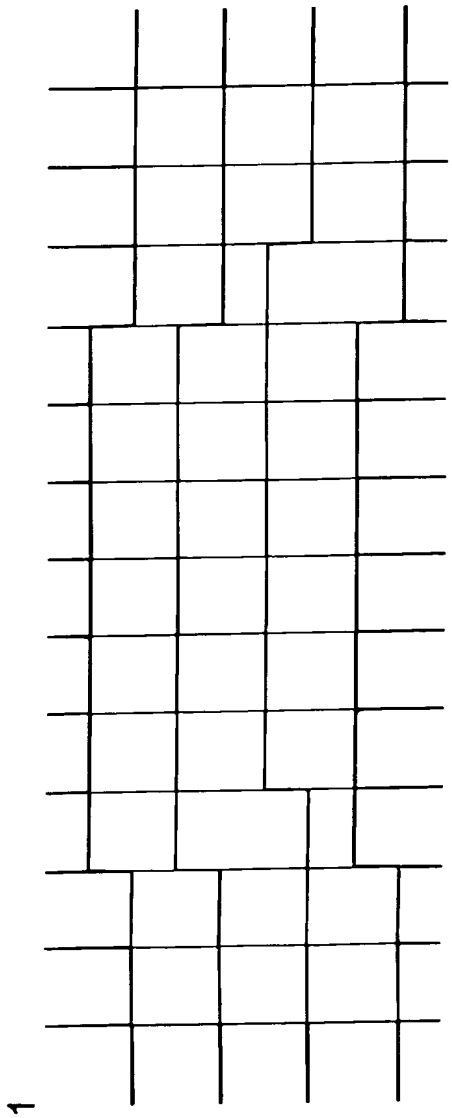

FIGURE 35B

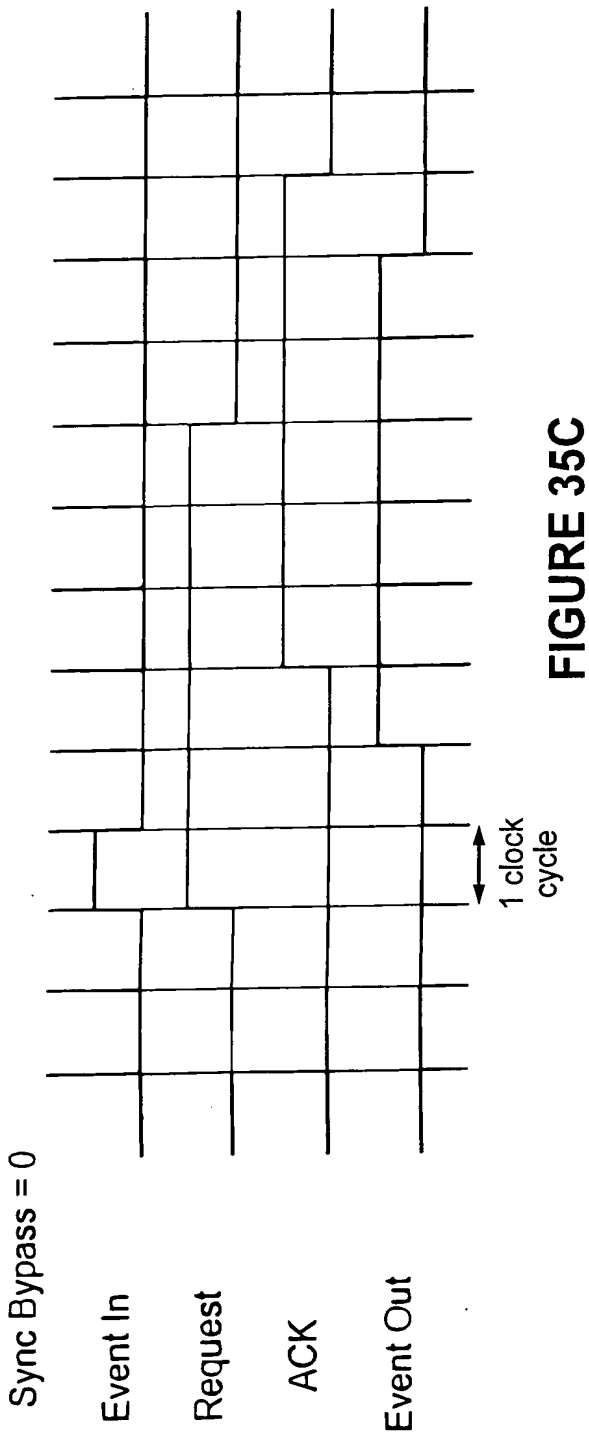

FIGURE 35C

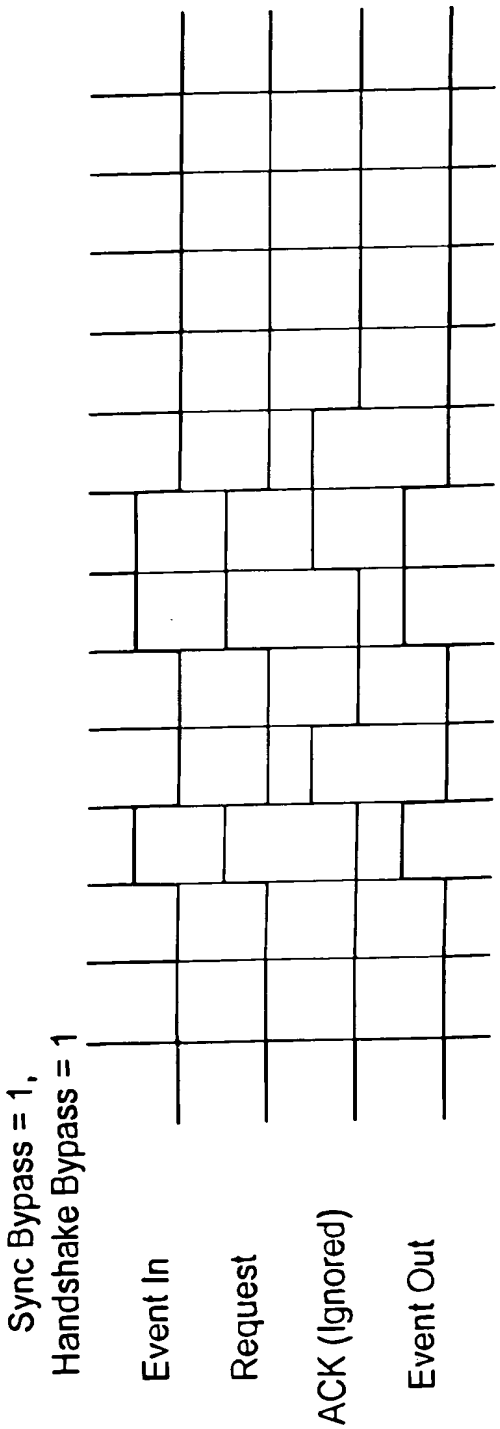

FIGURE 35D

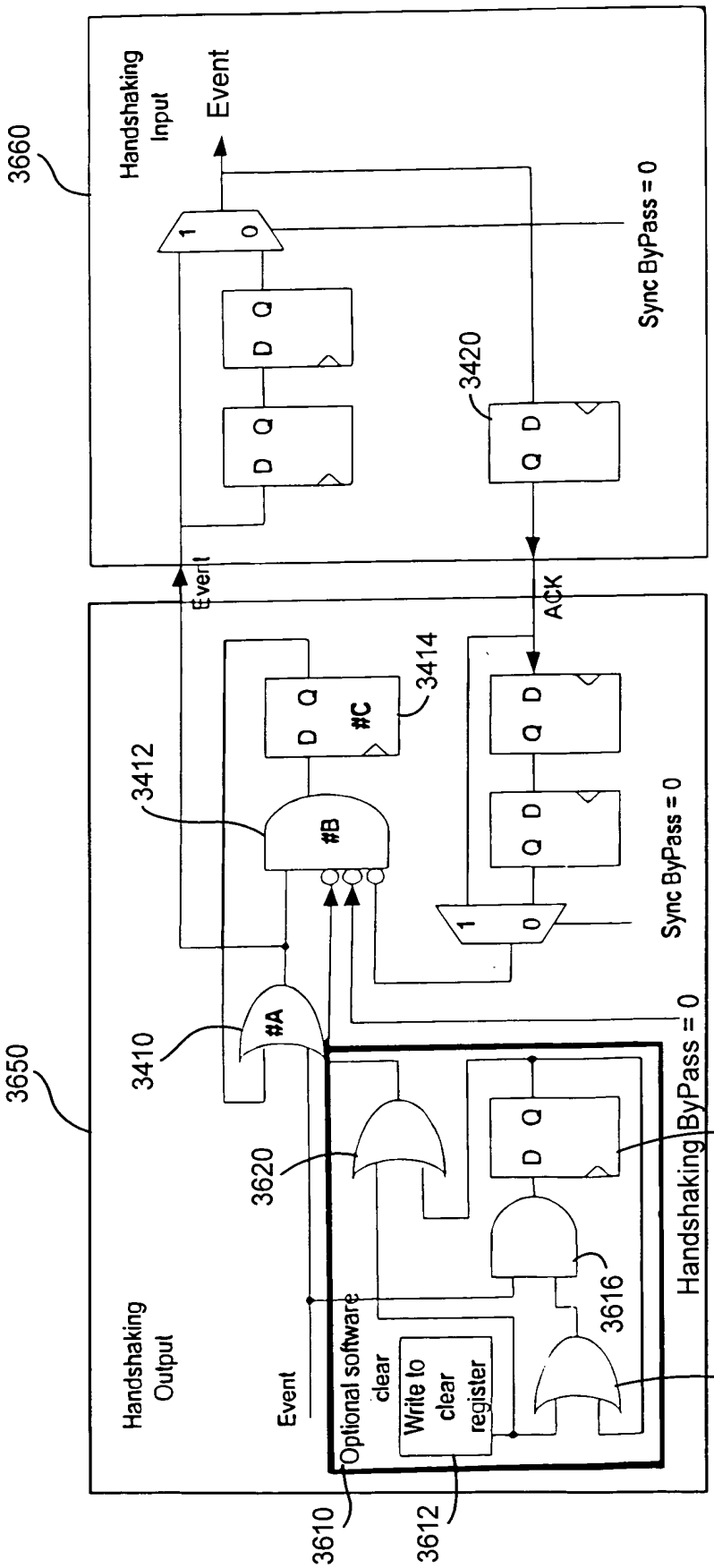
3660
Handshaking Input
Event
1
0
D Q
D Q
3420
Q D
Sync ByPass = 0
Event
ACK
3650
3414
#C
3412
#B
Q D
Q D
1
0
Sync ByPass = 0
3410
#A
Handshaking ByPass = 0
3620
3618
3616
Handshaking Output
Event
Optional software clear
Write to clear register
3614
3610
3612

FIGURE 36

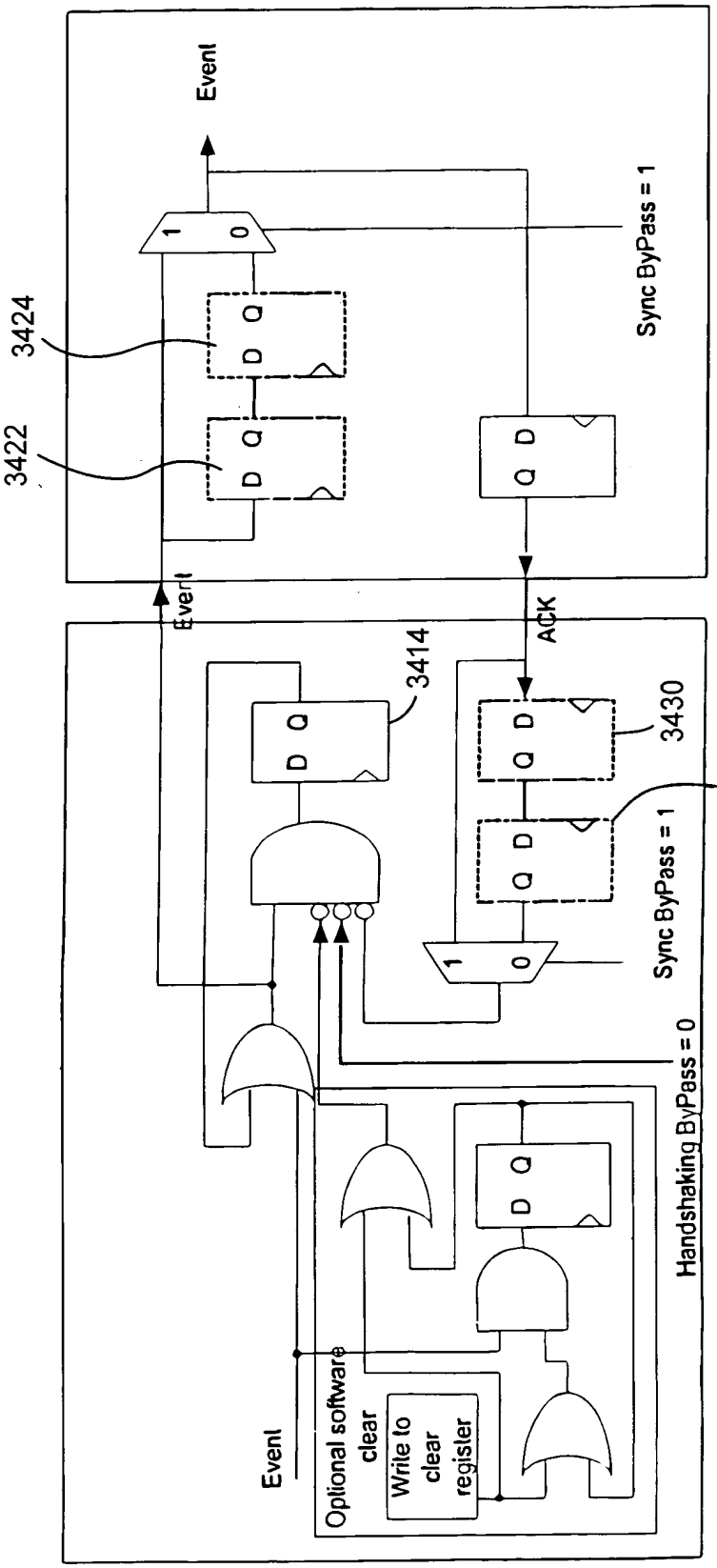
Event
Sync ByPass = 1
3424
3422
D Q
1
0
Event
ACK
3414
3430
3428
Sync ByPass = 1
Handshaking ByPass = 0
Event
Optional software clear
Write to clear register

FIGURE 37

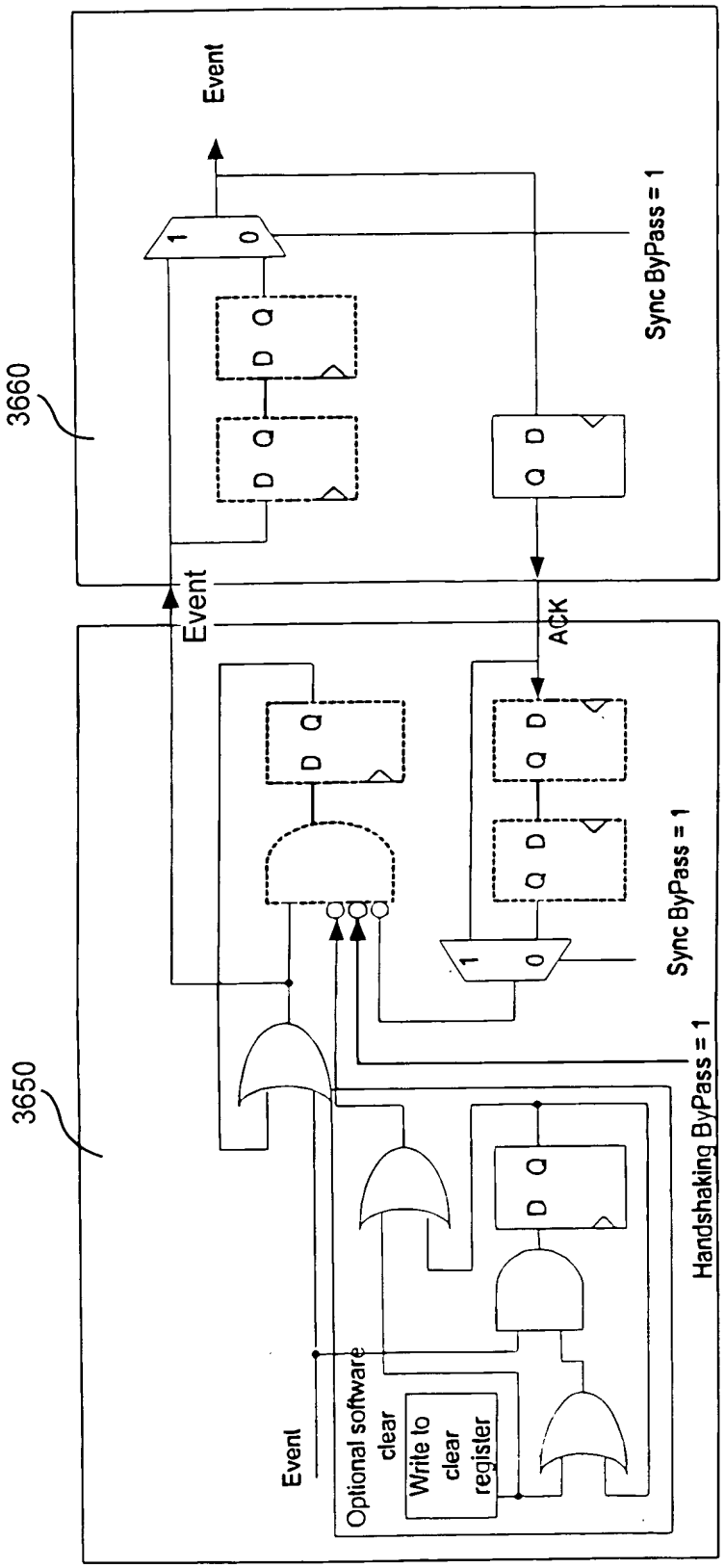
3660
Event
Sync ByPass = 1
Event
ACK
3650
Sync ByPass = 1
Handshaking ByPass = 1
Event
Optional software clear
Write to clear register

FIGURE 38

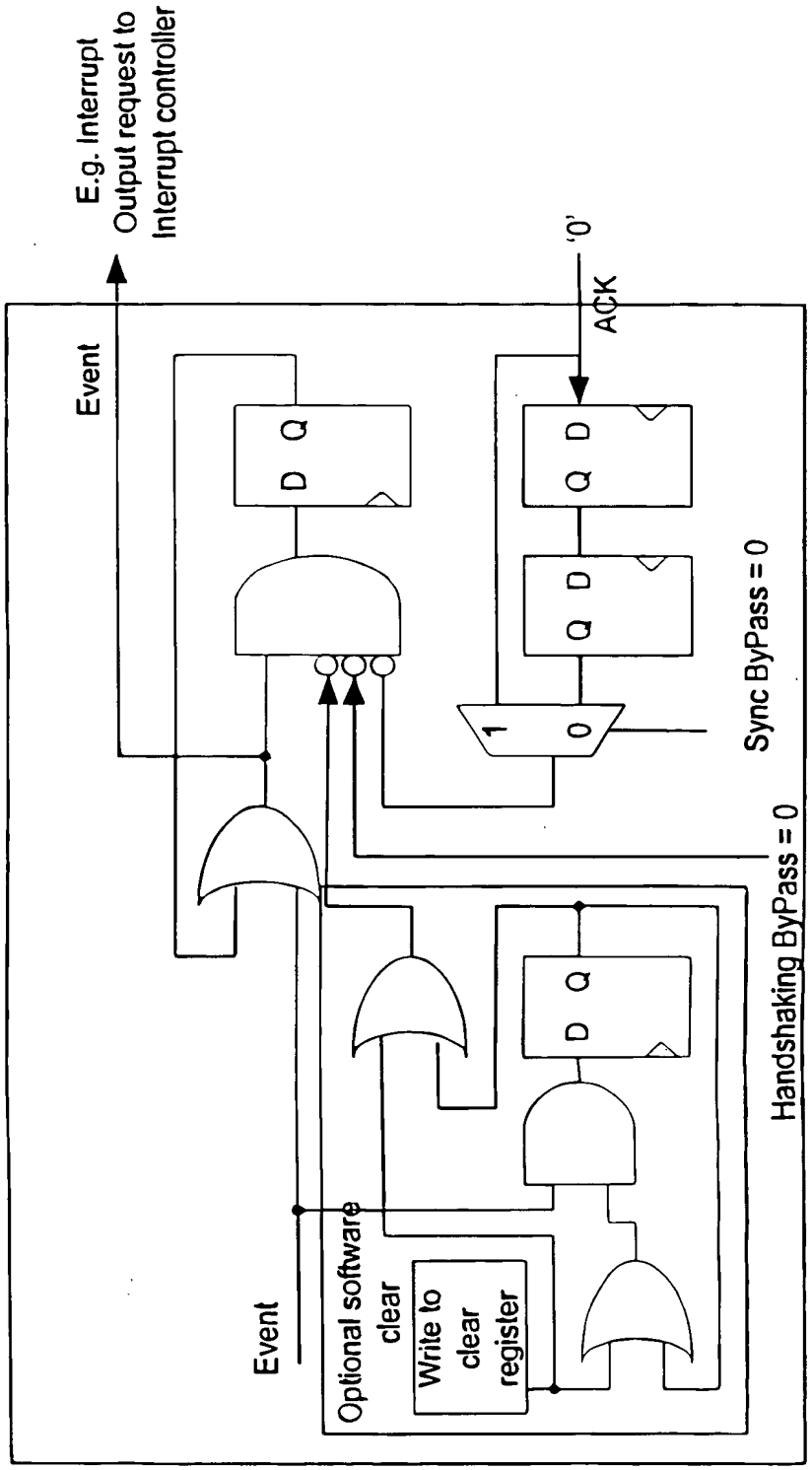
E.g. Interrupt
Output request to
Interrupt controller
Event
'0'
ACK
D Q
Q D
Q D
Sync ByPass = 0
1
0
Handshaking ByPass = 0
D Q
Event
Optional software
clear
Write to
clear
register

FIGURE 39

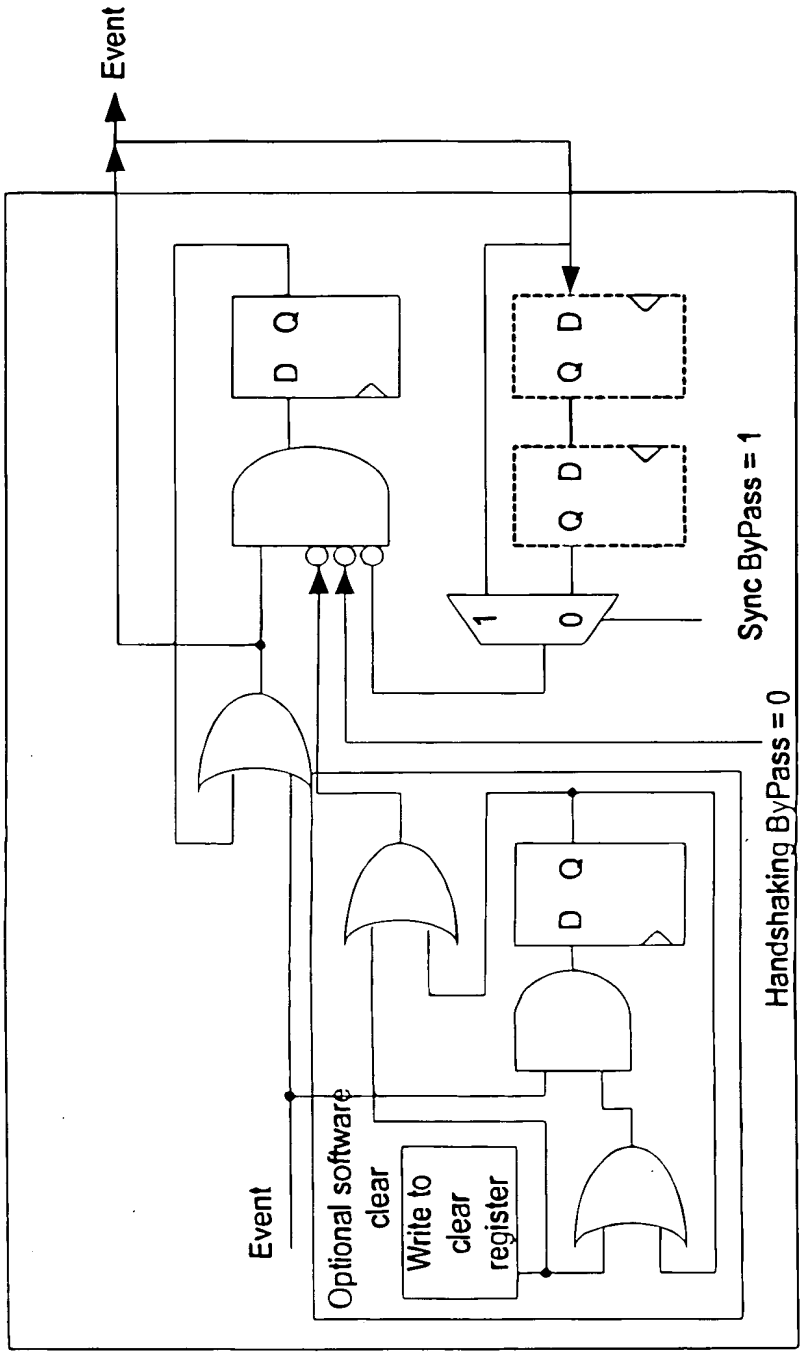
Event
D Q
D Q
D Q
D Q
1
0
Sync ByPass = 1
Handshaking ByPass = 0
D Q
Event
Optional software clear
Write to clear register

FIGURE 40

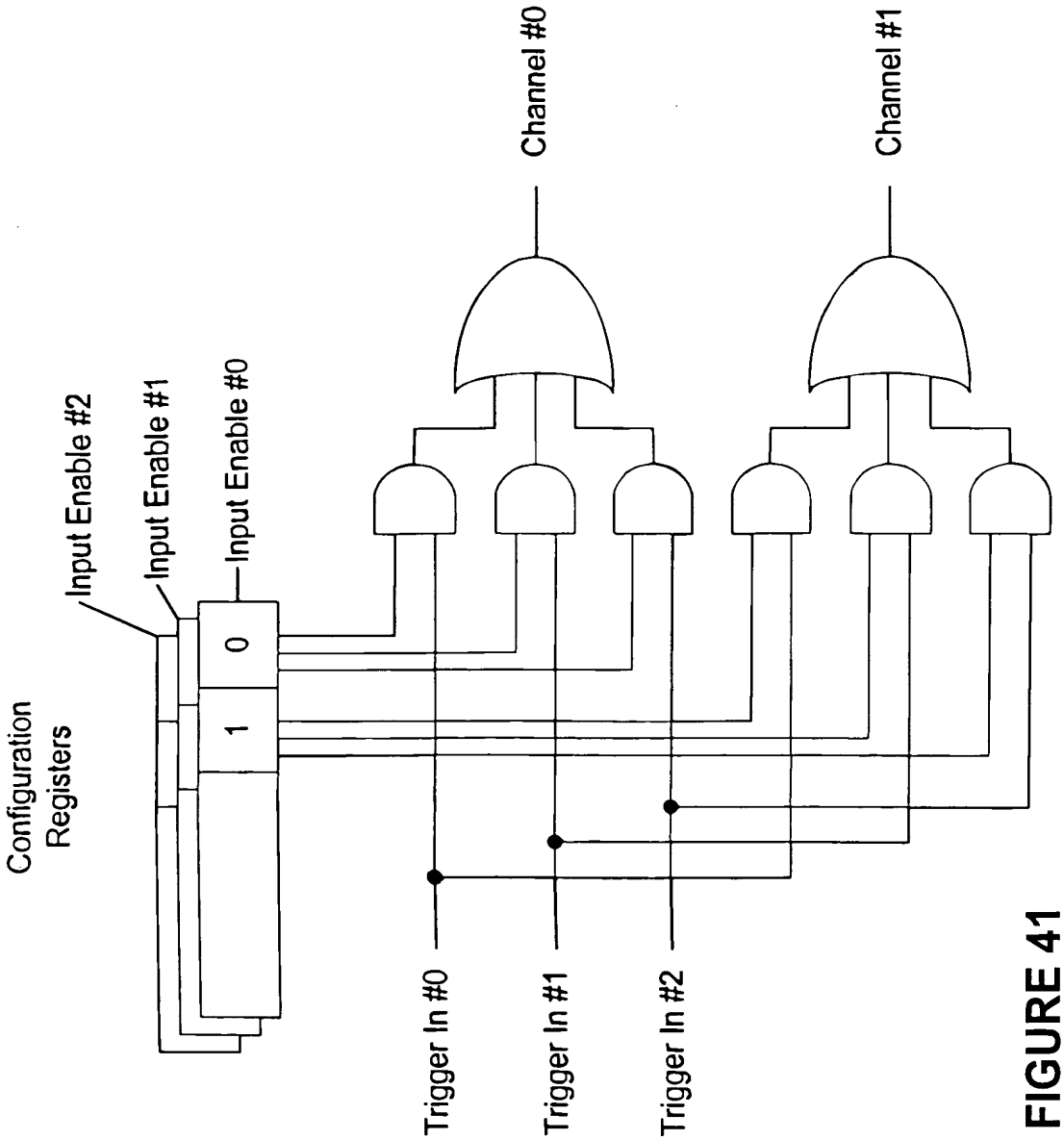
Channel #0
Channel #1
Input Enable #2
Input Enable #1
Input Enable #0
Configuration Registers
0
1
Trigger In #0
Trigger In #1
Trigger In #2

FIGURE 41

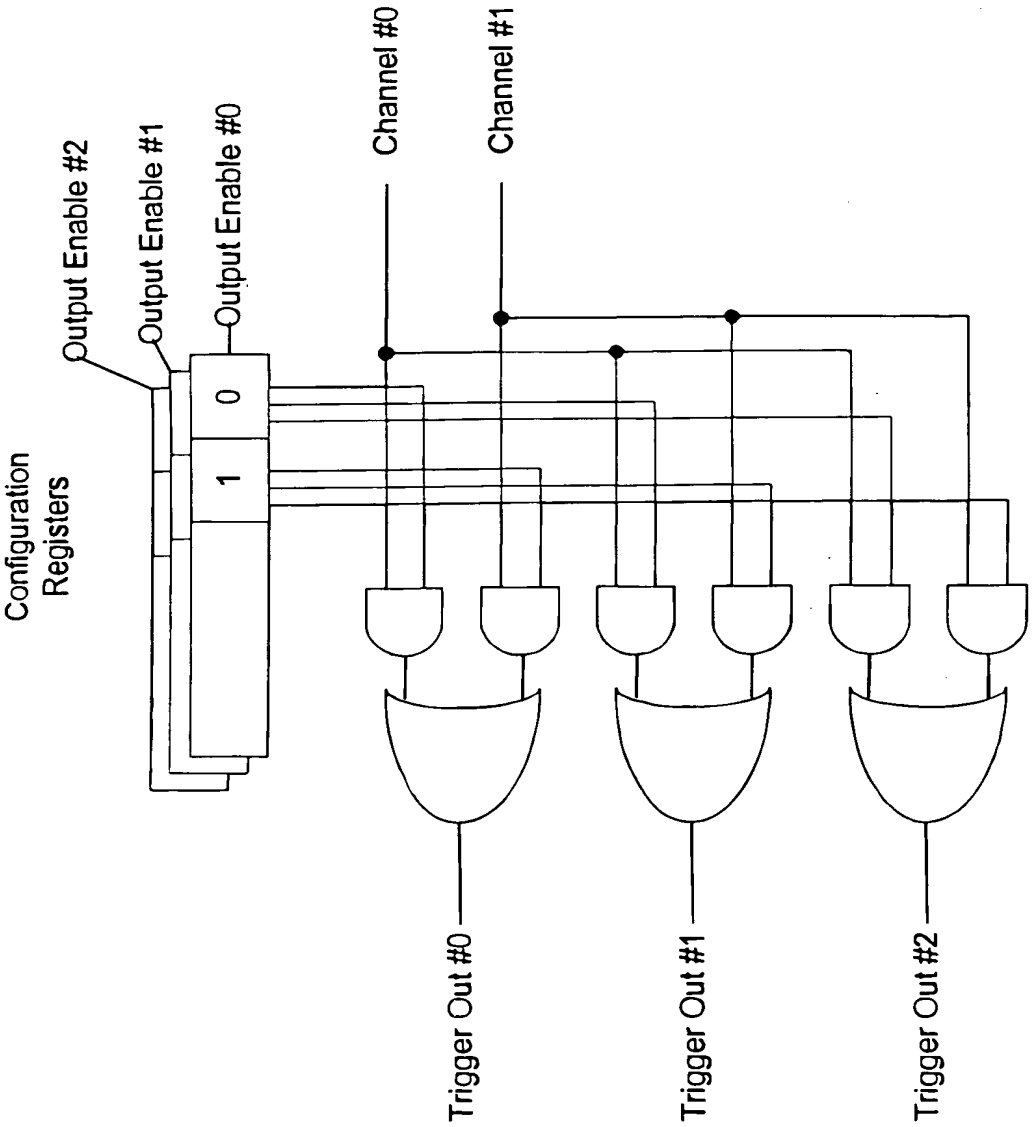
Configuration Registers
Output Enable #2
Output Enable #1
Output Enable #0
0
1
Channel #0
Channel #1
Trigger Out #0
Trigger Out #1
Trigger Out #2

FIGURE 42

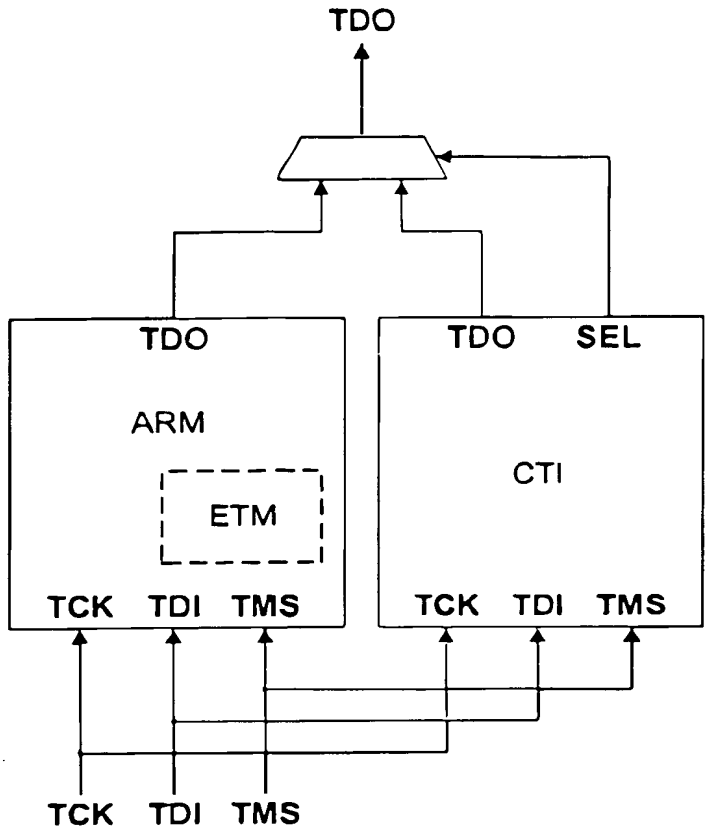

FIGURE 43

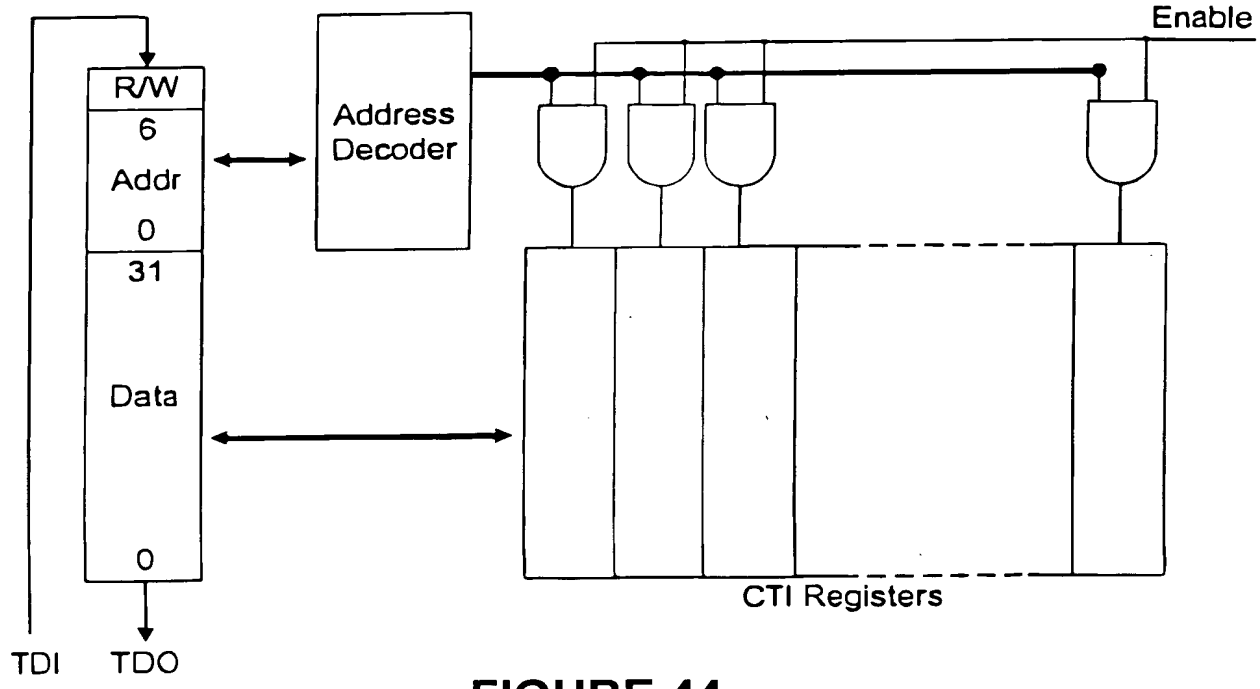

FIGURE 44

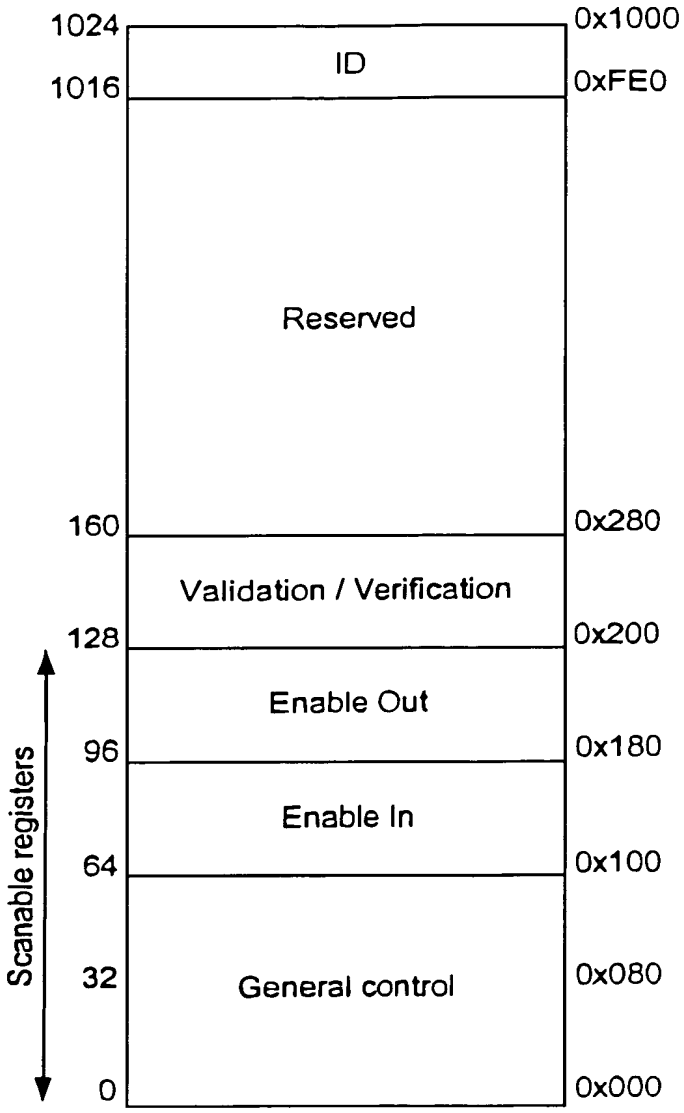
1024
0x1000
ID
1016
0xFE0
Reserved
160
0x280
Validation / Verification
128
0x200
Enable Out
96
0x180
Enable In
64
0x100
General control
32
0x080
0
0x000
Scanable registers

FIGURE 45A

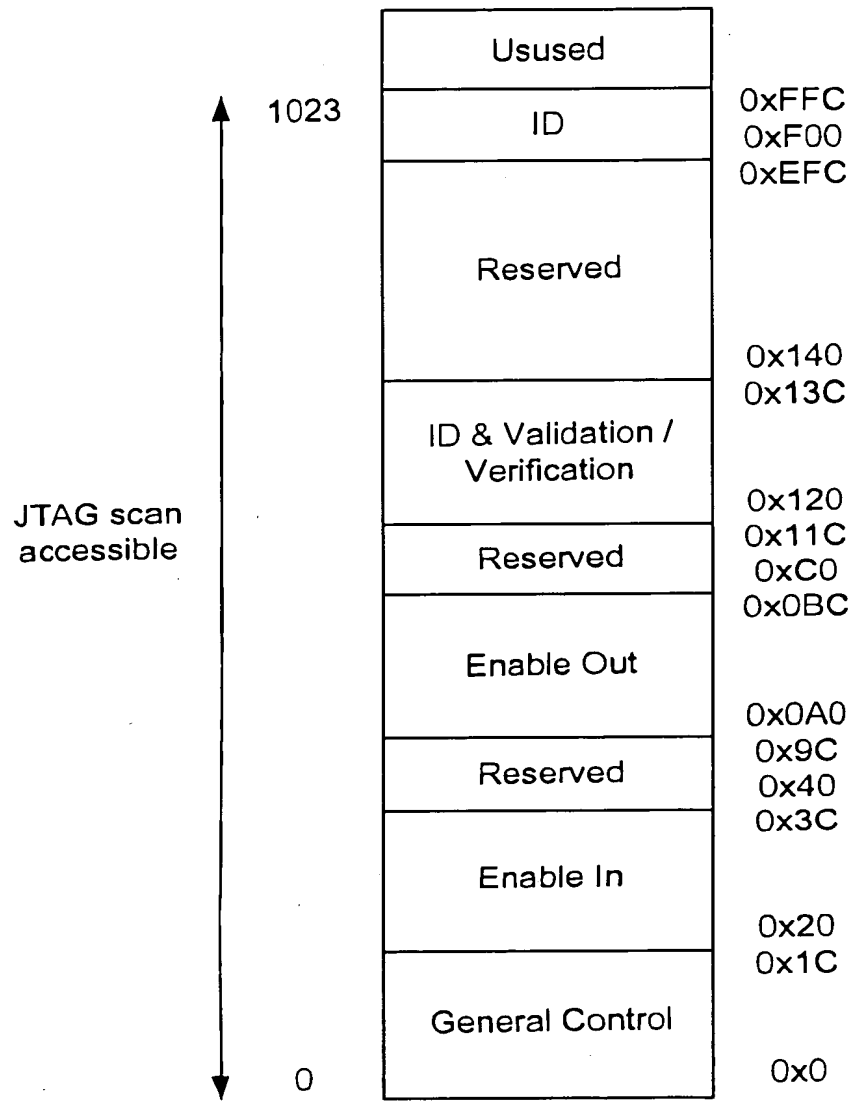
Ususued
ID
Reserved
ID & Validation / Verification
Reserved
Enable Out
Reserved
Enable In
General Control
1023
0
JTAG scan accessible
0xFFC
0xF00
0xEFC
0x140
0x13C
0x120
0x11C
0xC0
0x0BC
0x0A0
0x9C
0x40
0x3C
0x20
0x1C
0x0

FIGURE 45B

CTGENCTL	(0x000)	R - R/W

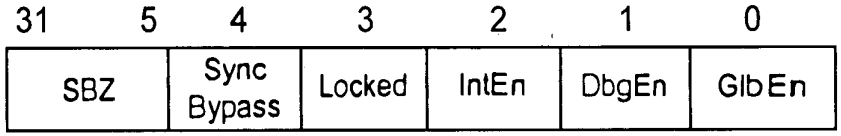

FIGURE 46

CTLOCK	(0x004)	R/W

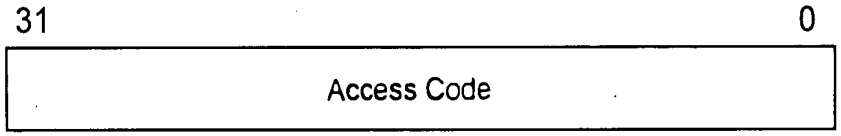

FIGURE 47

CTINTRAWSTATUS	(0x008)	R

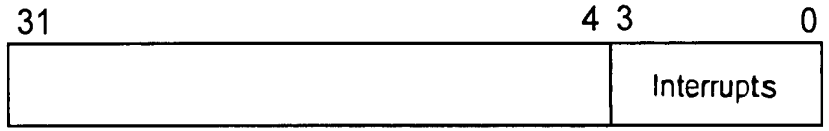

FIGURE 48

CTINTSTATUS	(0x00C)	R

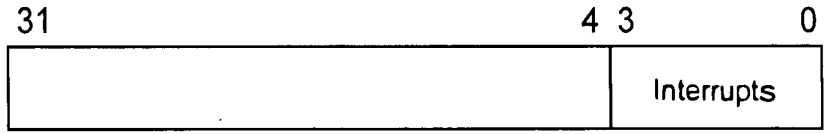

FIGURE 49

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CTINTCLEAR	(0x010)	W

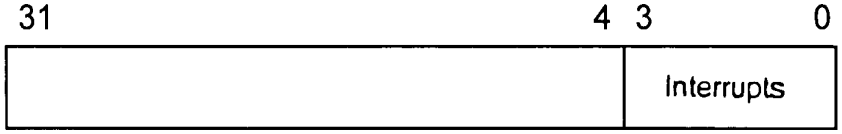

FIGURE 50

CTAPPTRIG	(0x080)	R/W

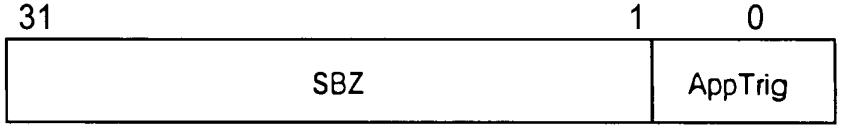

FIGURE 51

CTPERIPHID	(0x0E0)	R

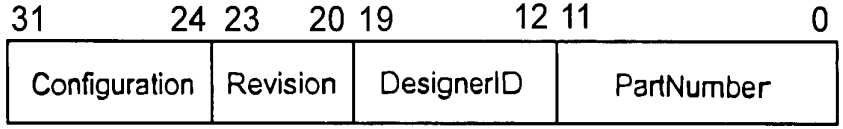

FIGURE 52

CTCHANNELSDEF	(0x0E4)	R

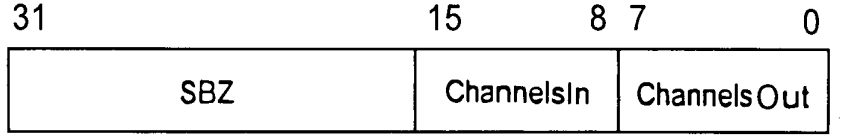

FIGURE 53

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CTINPUTSDEF	**(0xE8)**	**R**

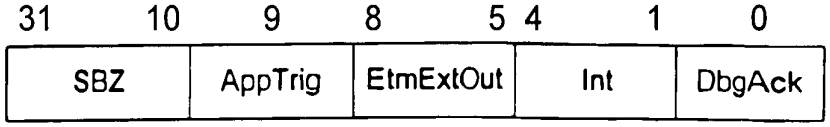

FIGURE 54

CTOUTPUTSDEF	**(0xEC)**	**R**

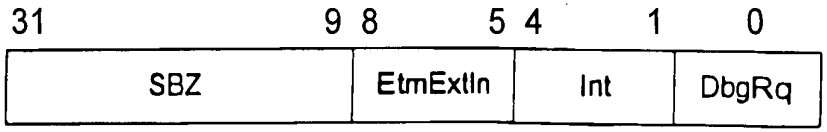

FIGURE 55

CTPCELLID	**(0x0F0)**	**R**

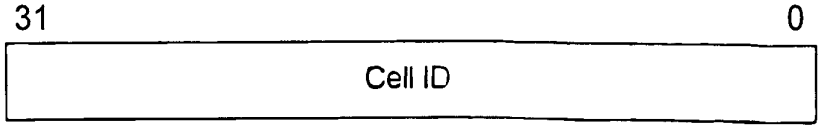

FIGURE 56

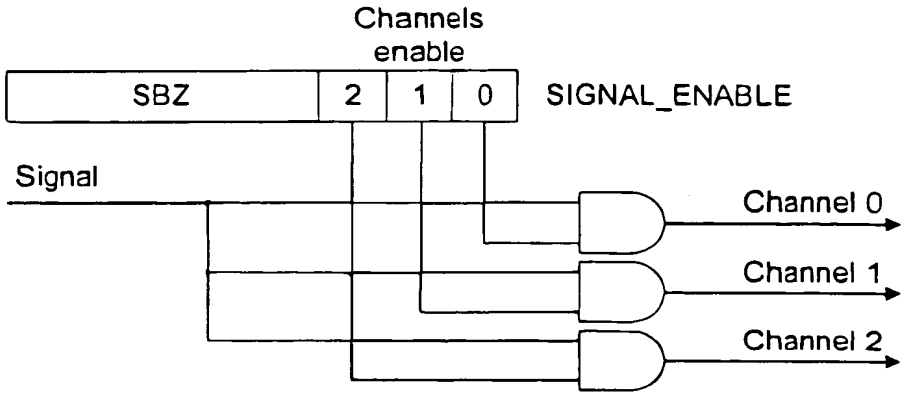

FIGURE 57

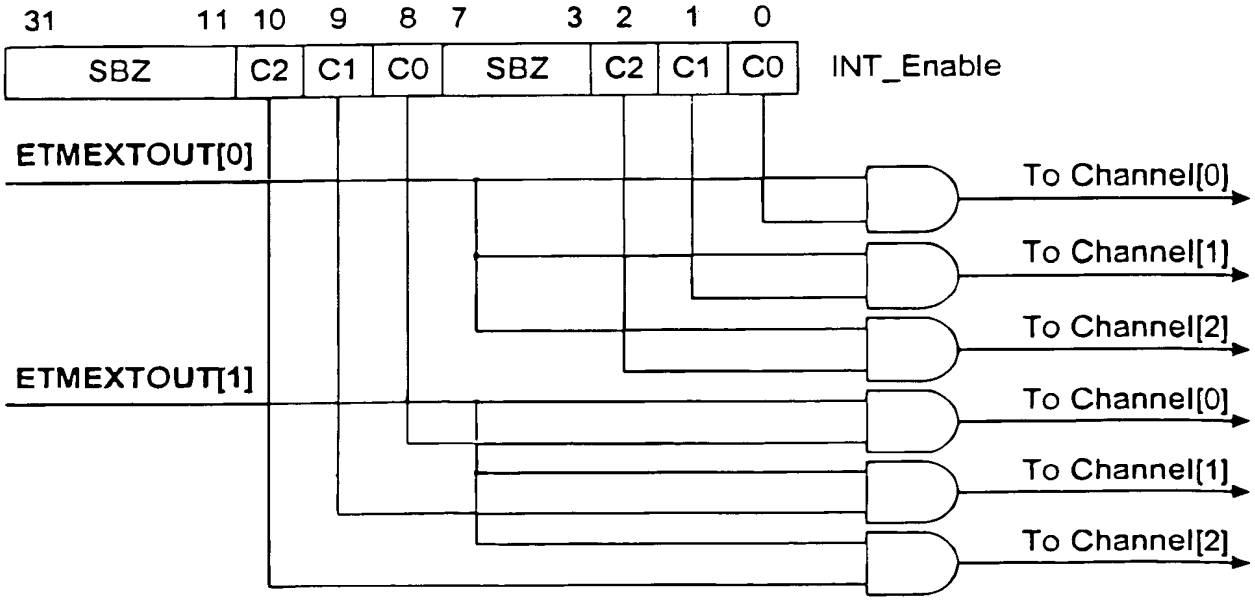

FIGURE 58

CTDBGACKEN	**(0x100)**	**R/W**

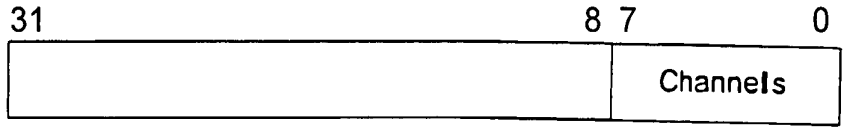

FIGURE 59

CTINTINEN	**(0x104)**	**R/W**

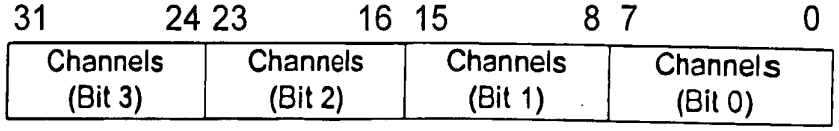

FIGURE 60

CTETMEXTOUTEN	**(0x108)**	**R/W**

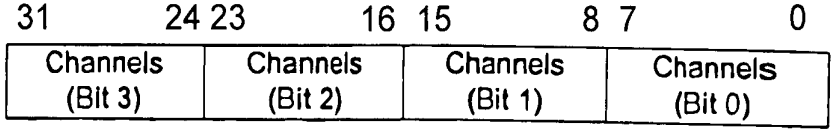

FIGURE 61

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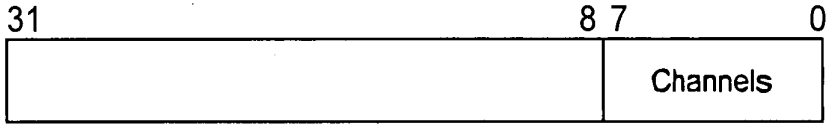
CTAPPTRIGEN	(0x110)	R/W	

FIGURE 62

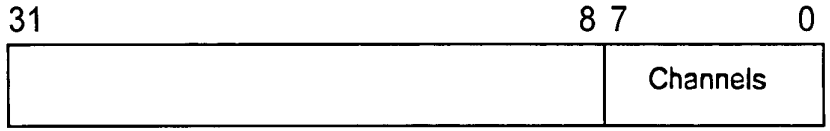
CTDBGRQEN	(0x180)	R/W	

FIGURE 63

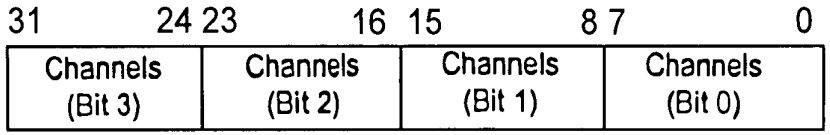
CTINTOUTEN	(0x184)	R/W	

FIGURE 64

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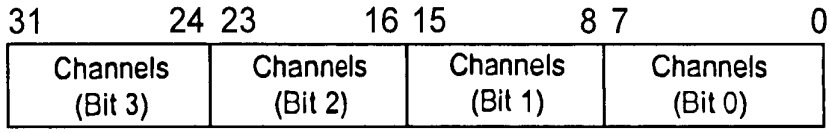
CTETMEXTINEN	(0x188)	R/W	

FIGURE 65

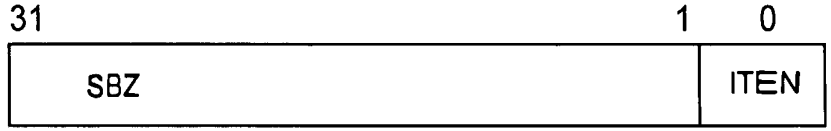
CTITCR	(0x200)	R/W	

FIGURE 66

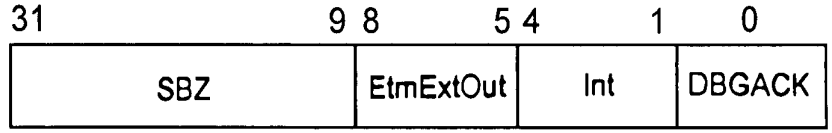
CTITIP1	(0x204)	R/W	

FIGURE 67

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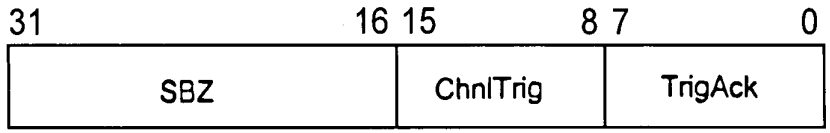
CTITIP2	(0x208)	R/W	

FIGURE 68

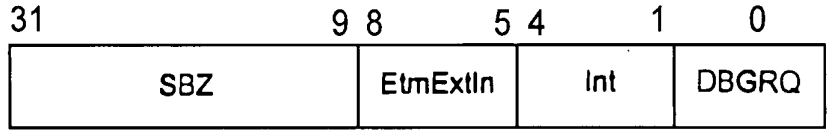
CTITOP1	(0x20C)	R/W	

FIGURE 69

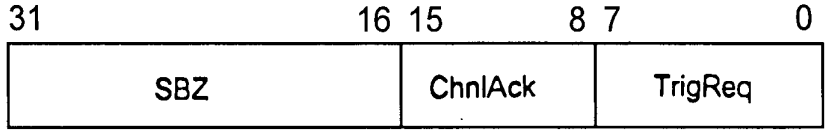
CTITOP2	(0x210)	R/W	

FIGURE 70

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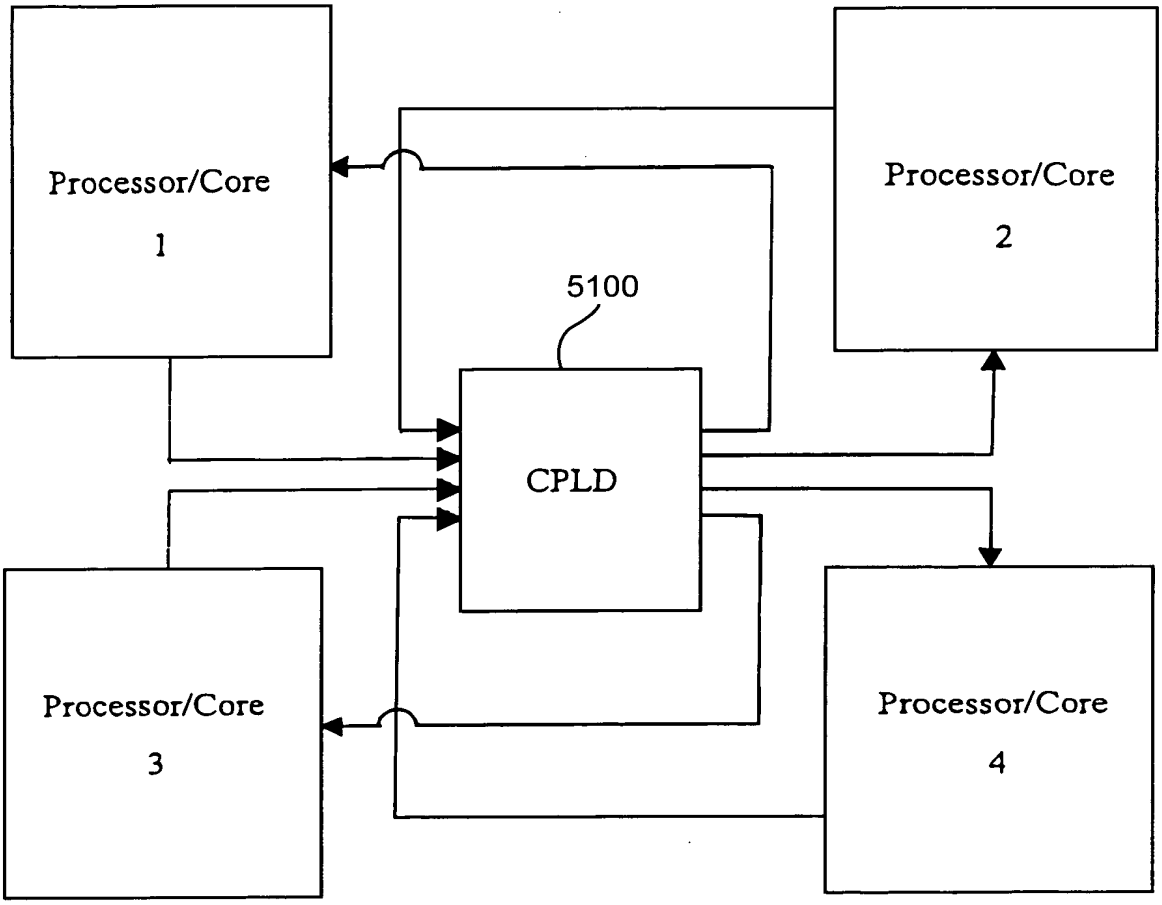

FIGURE 71
PRIOR ART

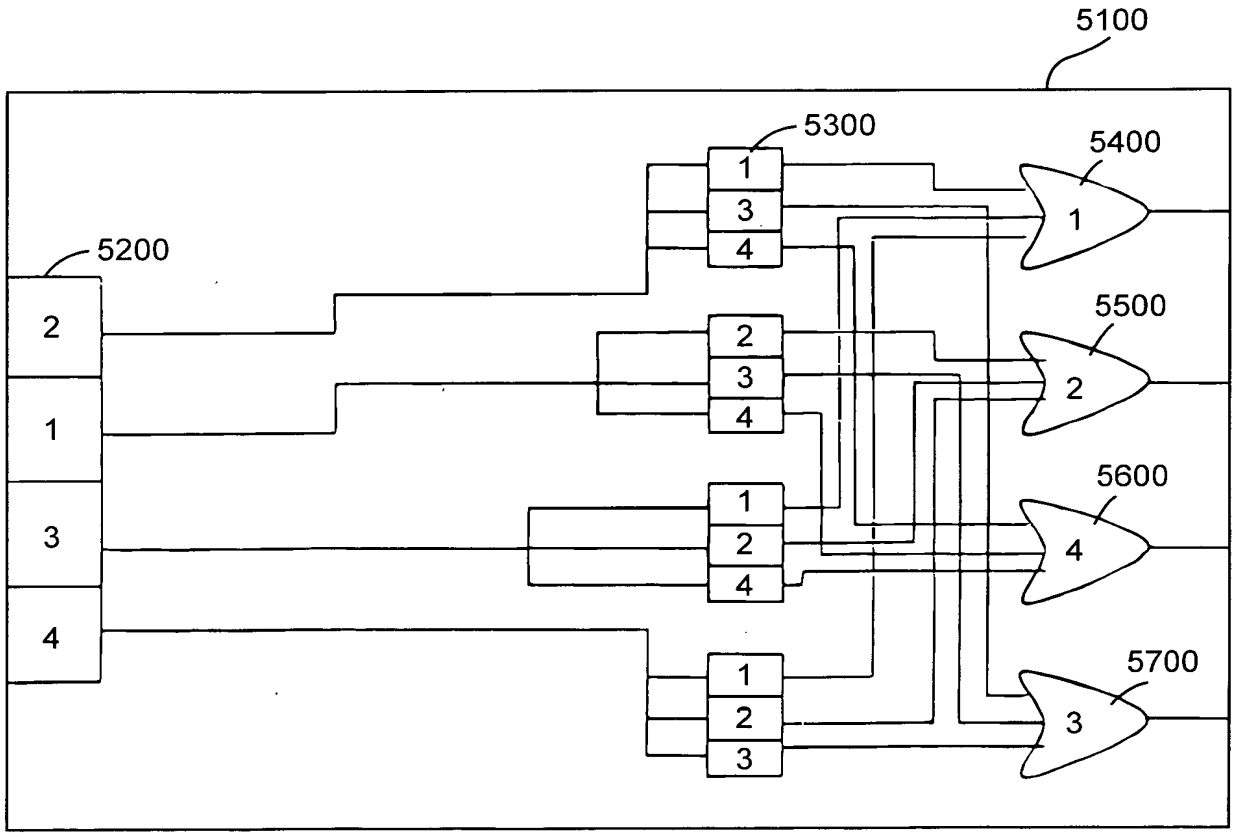

FIGURE 72
PRIOR ART